# The MARCO/DARPA Gigascale Silicon Research Center Overview and Progress Report

GSRC

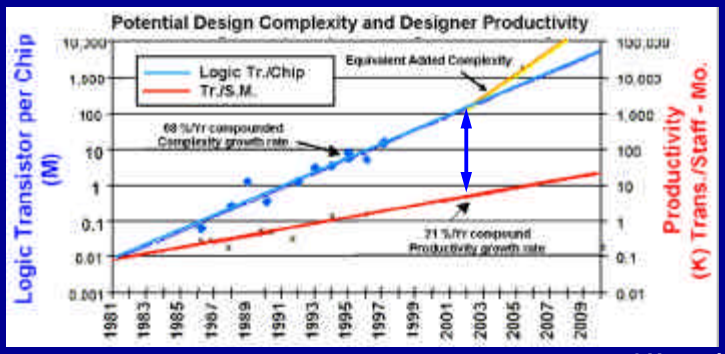
DARPA Kickoff Workshop
Washington, DC
December 6th, 2001

SIA Semiconductor Industry Suppliers

DUSD(S&T)

DARPA

## The Productivity Gap




| Year | Technology | Chip Complexity | Frequency | Staff | 3 Yr. Design Staff Cost* |
|---|---|---|---|---|---|
| 1997 | 250 nm | 13 M Tr. | 400 MHz | 210 | 90 M |
| 1998 | 250 nm | 20 M Tr. | 500 | 270 | 120 M |
| 1999 | 180 nm | 32 M Tr. | 600 | 360 | 160 M |
| 2002 | 130 nm | 130 M Tr. | 800 | 800 | 360 M |

GSRC

* @ $ 150 k / Staff Yr. (In 1997 Dollars)

Source: SEMATECH

## Implications of *Not* Doing the Research

- If we do not solve these long-lead-time problems:
  - Accelerated slowdown in design productivity
  - Increasing unpredictability in design cycle
  - Inability to verify/correct complex designs
  - Major NRE cost increase for complex designs (likely anyway!)
- Which leads to:
  - Expensive chips—large markets economically inaccessible
  - Inability to guarantee hitting market window
  - Quality issues in the field

Overall industry slowdown

GSRC

## "It's a Moonshot, Not Rocket Science"

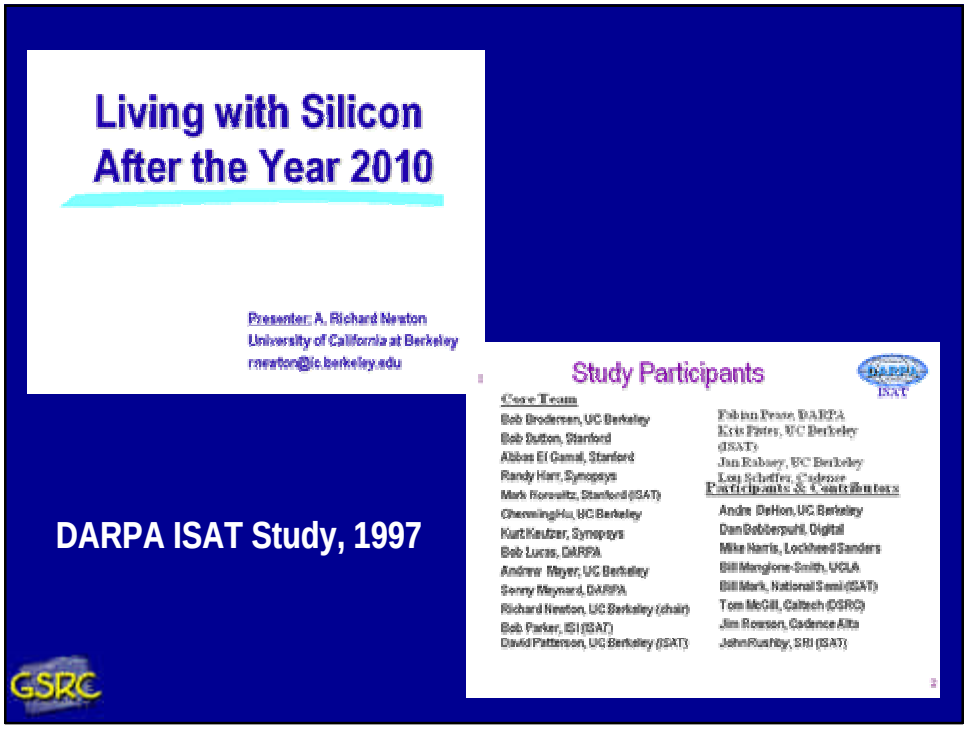
**Overall Program Goals**

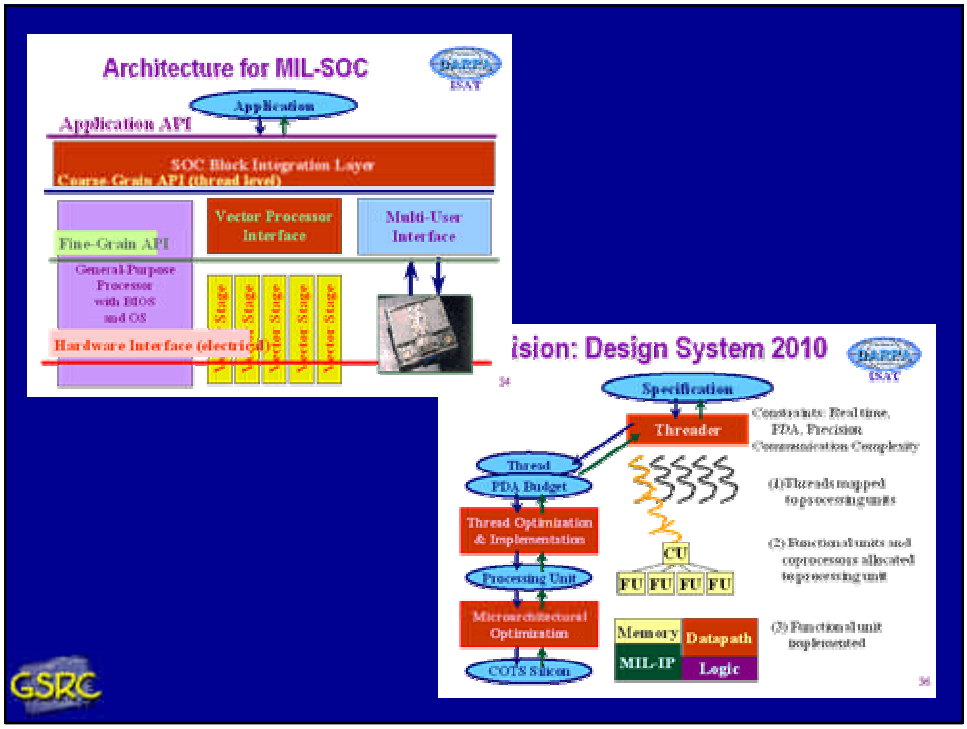
- > 1 Billion transistor chip
- In a technology < 35nm
- Using IP from several sources (mixed-signal)
- Running at >20GHz on-chip
- With a team of < 30 designers
- In < 6 months
- With competitive cost and power-delay-area product

Proposed GSRC 10-Year Goal, November 1997

Motivated by "Grand Challenge" Problems

GSRC




# What Would "Success" Look Like?

- Design implementation with predictable, microprocessor-quality components on an ASIC schedule
  - Emphasis on efficient, predictable, cost-effective component implementation strategies
  - Role of reuse and communication-based assembly and verification approaches
  - Emphasize energy and power management
- Building highly-reliable systems from unreliable/unpredictable components and technologies
  - Accurate statistical characterization of process and its circuit-level implications
  - New circuit design styles to accommodate the above
  - Integration with test, diagnosis and self-repair, including analog

GSRC

GSRC 10-Year Goal, March 1999

## What Would "Success" Look Like?

- Enable programmable solutions through programming support for complex, programmable IC's
  - A natural programmer's model that allows for efficient utilization of the platform for a variety of applications
  - Emphasis on exploiting and managing concurrency in the application and its implementation
- Develop a solution (methodology and technologies) for the effective and reliable exploitation of concurrency in the design and correct implementation of hardware and software-based single-chip systems and their interfaces

GSRC

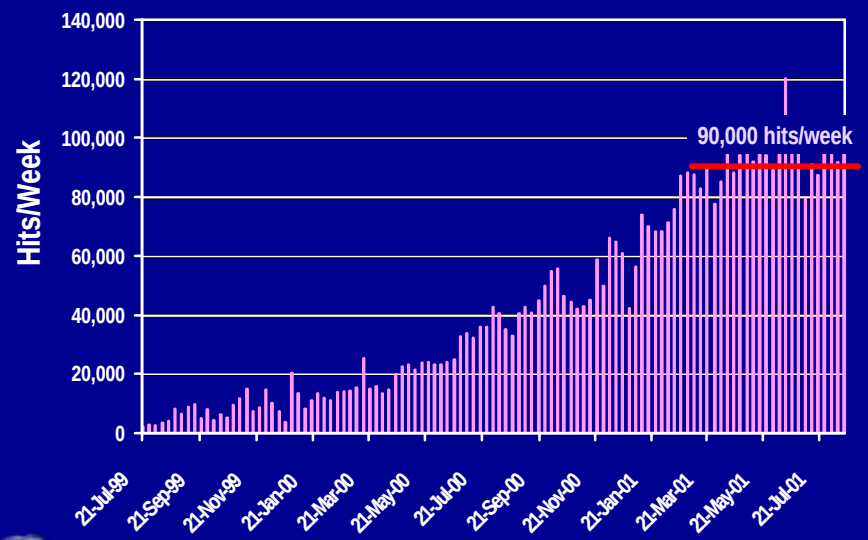
GSRC 10-Year Goal, March 1999

## www.gigascale.org : A Critical and Effective Resource

- Example: August 2001
  56,541 accesses
  - 400,841 hits
  - Average visit 3 pages
  - Served 755 Mbytes
  - Broad range of users:
    - 29% from *com*
    - 9.2% from *edu*
    - 1% from *mil, gov*
    - 21% overseas: 63 countries
      - France, Canada, Finland, Netherlands, Germany, Hong Kong, Japan heaviest visitors


GSRC

## GSRC Website Statistics: July 1999 – August 2001




GSRC

## The Gigascale Silicon Research Center

http://www.gigascale.org

**"Empowering designers
to realize the potential of gigascale silicon by enabling
scaleable, heterogeneous, component-based design
with a
single-pass route to efficient
silicon implementation from a microarchitecture"**

GSRC

## Overarching GSRC Research Emphasis for 2001—…? :

"From Ad-Hoc System-on-a-Chip Design to Disciplined, Platform-Based Design"

GSRC

## The Gigascale Silicon Research Center

http://www.gigascale.org

"Empowering designers
to move from ad-hoc system-on-a-chip design
to disciplined, platform-based design by enabling
scaleable, heterogeneous, component-based design
with a
single-pass route to efficient
silicon implementation from a microarchitecture"

GSRC

# What is a Platform?

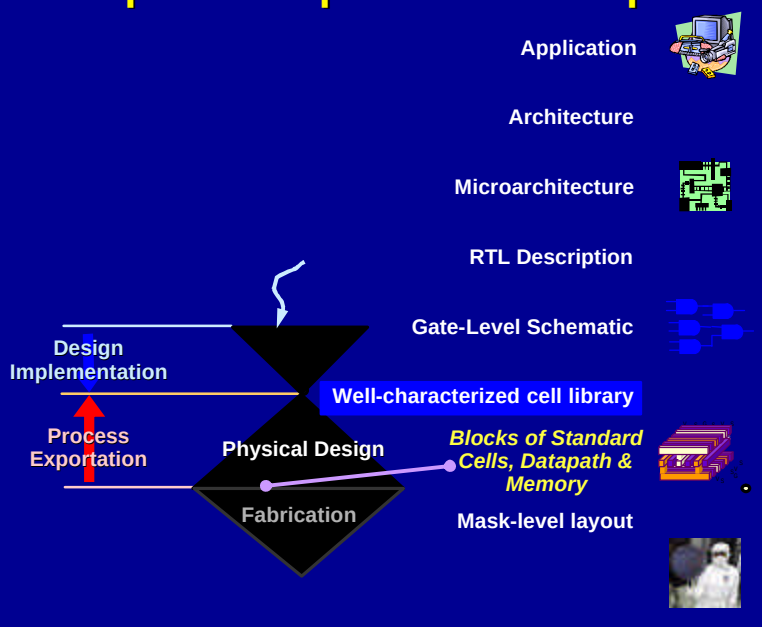
- Broadly stated, a Platform is a restriction on the space of possible implementation choices, providing a well-defined abstraction of the underlying technology for the application developer
- A Platform is a coordinated family of hardware-software architectures, that satisfy a set of architectural constraints, imposed to allow the re-use of well-characterized hardware and software components and technologies.
- New platforms will be defined at the architecture-microarchitecture boundary
- They will be heterogeneous and component-based, and will provide a range of choices from structured-custom to fully programmable implementations

"Only the consumer gets freedom of choice; designers need freedom *from* choice"
(Orfali, et al, 1996, p.522)

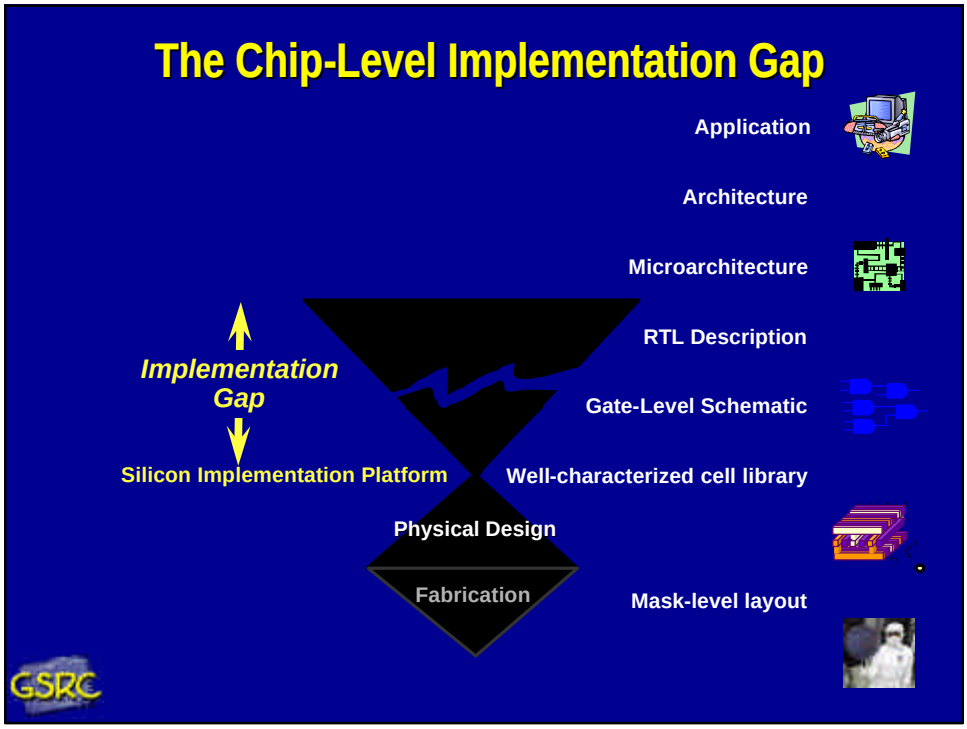
GSRC

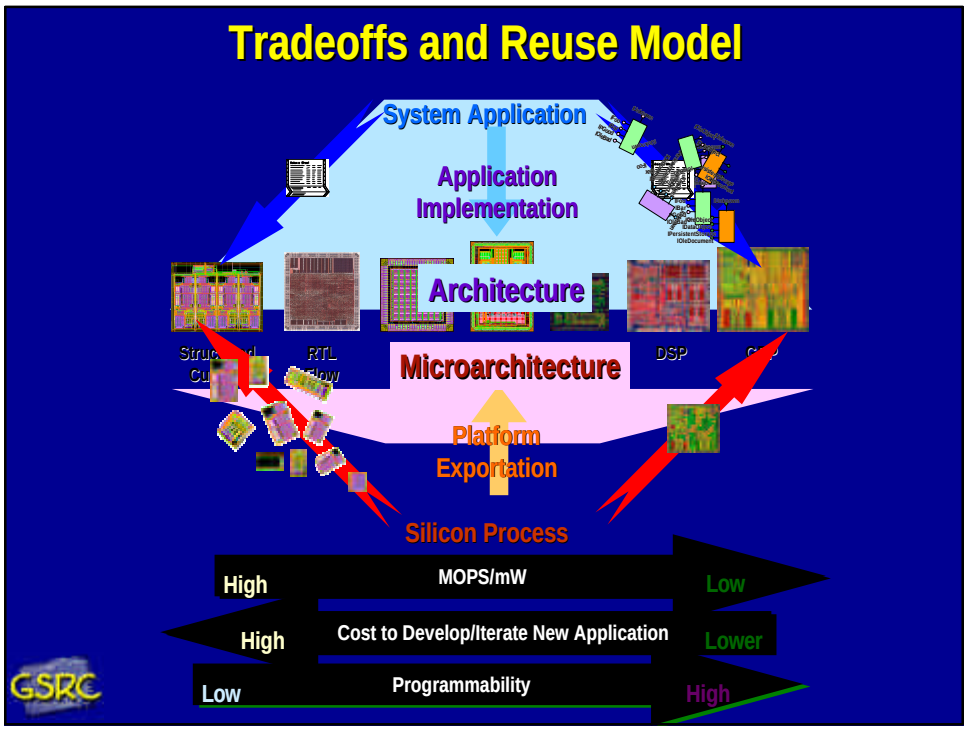
Contact: Alberto Sangiovanni

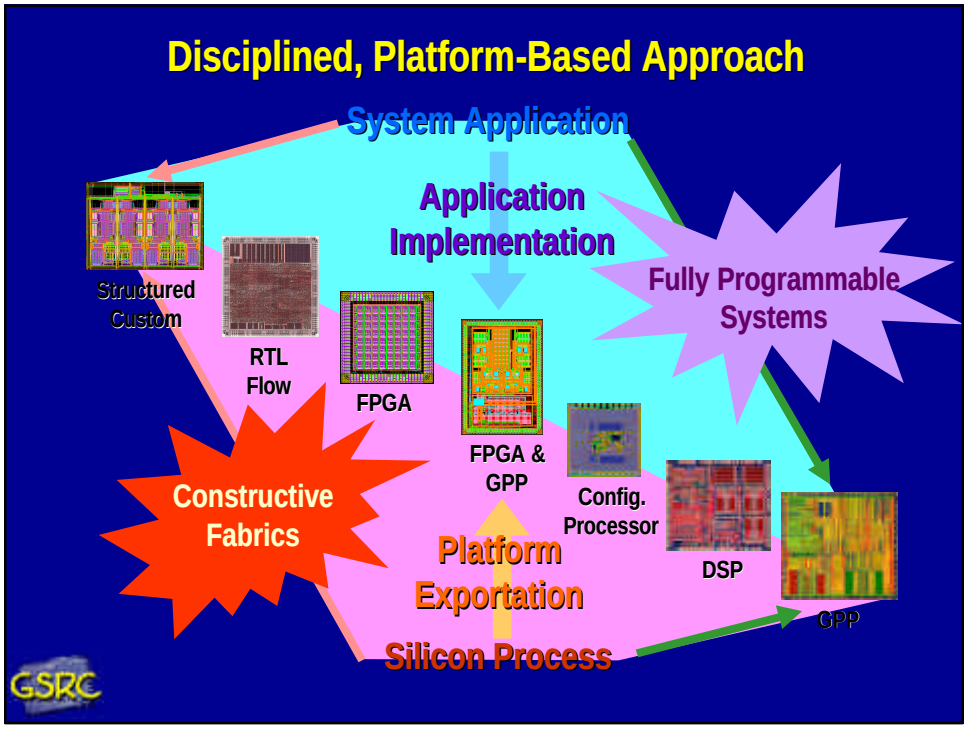
# The Chip-Level Implementation Gap




GSRC





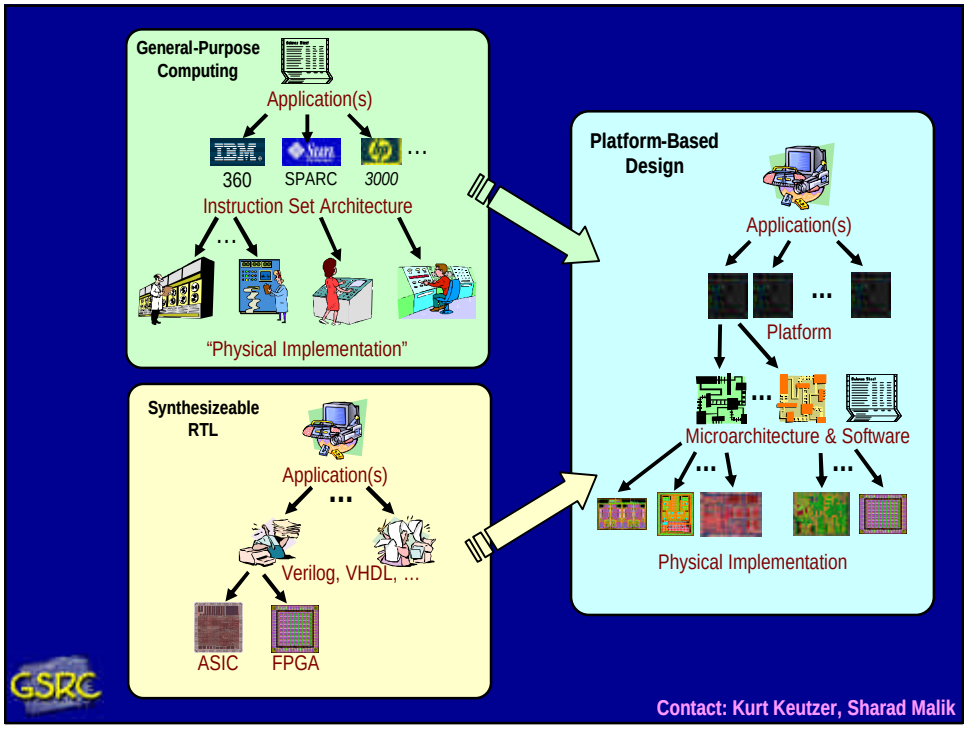

## Current Scenario–ASIPS on the Rise in Networking

| Company | Product | RISC based | Task Specific Processor based | ASIC |
|---|---|---|---|---|
| Level One | *IXP1200* | ✔ | | |
| IBM | *PNP* | ✔ | | |
| MMC | *nP* | ✔ | | |
| Maker | *MXT* | ✔ | | |
| Sitera | *PRISM IQ1200* | ✔ | | |
| EZChip | *NP-1* | ✔ | | |
| C-Port | *C-5 DCP* | ✔ | | |
| Agere | *PayloadPlus* | | ✔ | |
| Fast-chip | *PolicyEdge* | | ✔ | |
| Hi-fn | *7711, 7751* | | ✔ | |
| Xaqti | *TeraPower-CL* | | ✔ | |
| Broadcom | *StrataSwitch* | | ✔ | |
| Solidum | *PAX.port 1100* | | ✔ | |
| Netlogic | *Policy, CIDR* | | ✔ | |
| Switchcore | *CXE* | | ✔ | |
| Entridia | *Opera* | | | ✔ |

Source: GSRC MESCAL Group

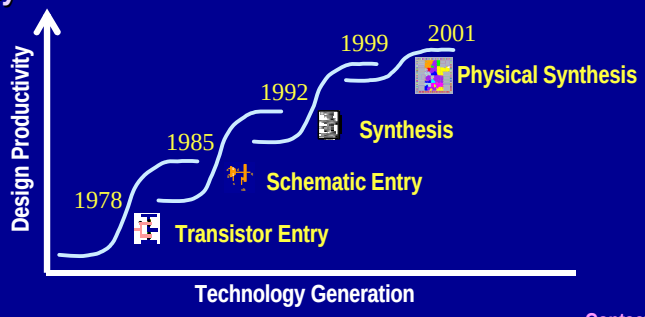
GSRC

Contact: Kurt Keutzer, Sharad Malik




## Regularity & Physical Design

- New design regularity has been the enabler for every quantum step in design automation and design productivity
- But DSM physical synthesis can not take us all the way to *affordable* gigascale w/o additional forms of regularity!
- Beyond MOSFETs, FINFETs, ..., we expect that logic patterns and implementation platforms will become more even regular—via self-assembly




GSRC

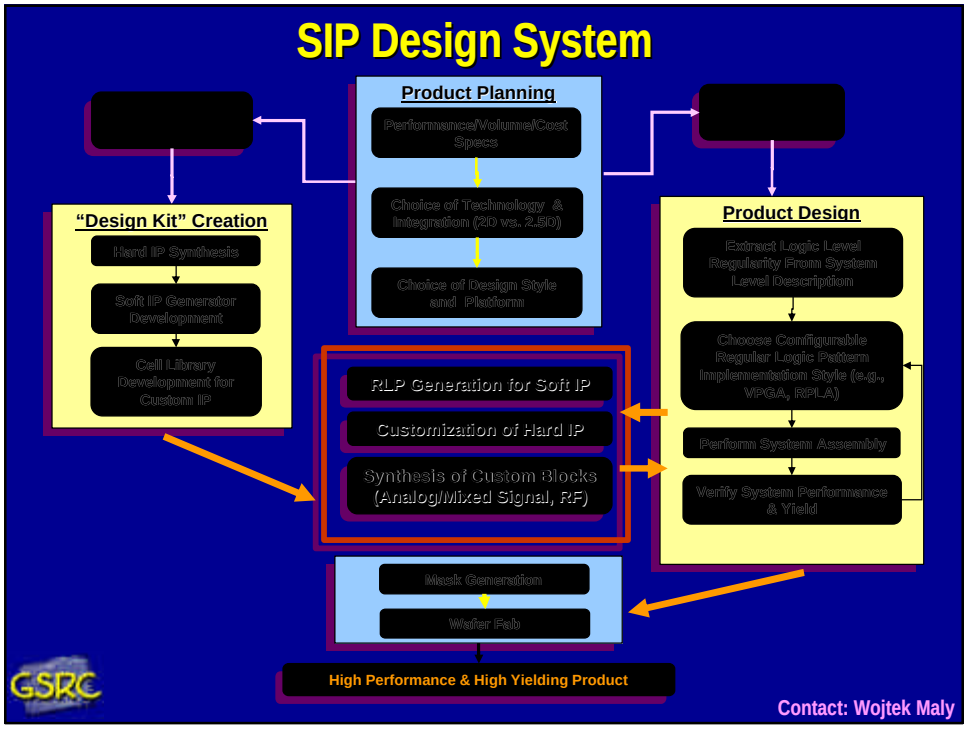
Contact: Larry Pileggi

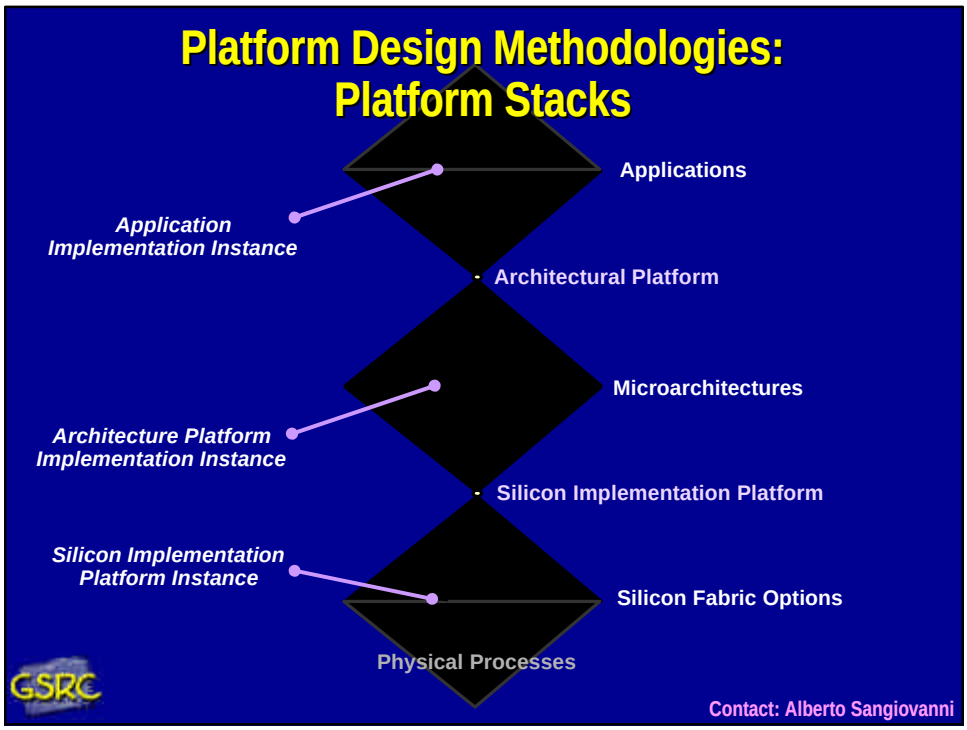
## DSM ASIC Implementation and Manufacturing

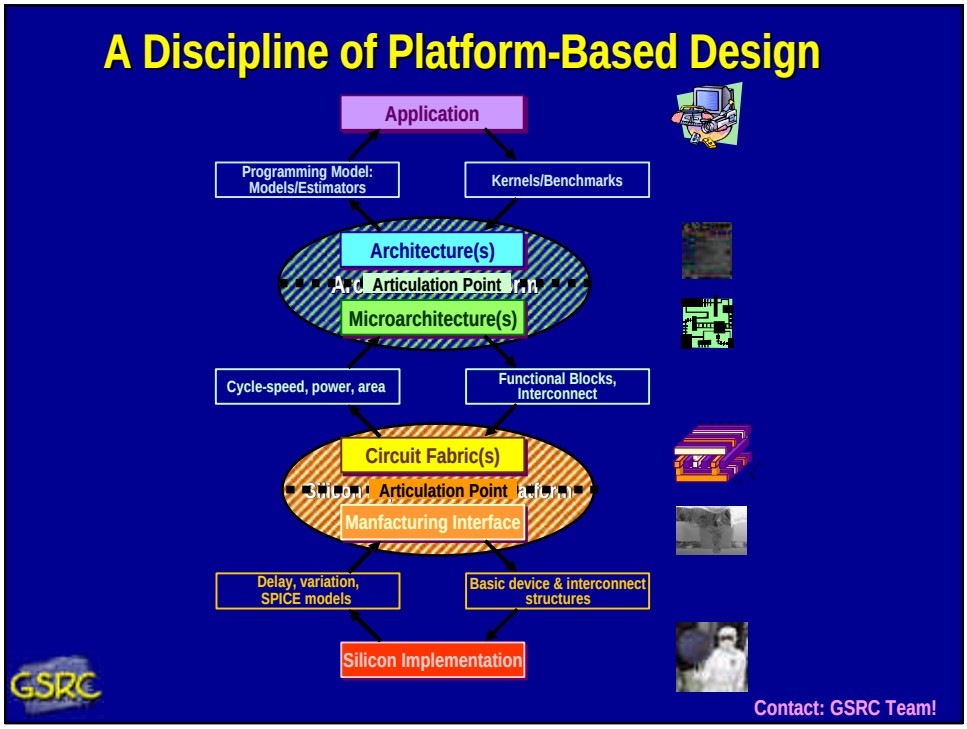
- Part of our research has been to understand, model and create forms of regularity to overcome DSM problems that include:
  - Printing and manufacturing high yield silicon with nanometer feature sizes
  - Creating reliable designs with component parameters that vary substantially
  - Distributing power reliably and guaranteeing signal integrity
  - Structured communication channels and/or clocking methodologies
  - Providing accurate prediction capabilities for system-level exploration from the Architectural Platform level
  - Facilitating reliable design signoff for guaranteed first-pass success

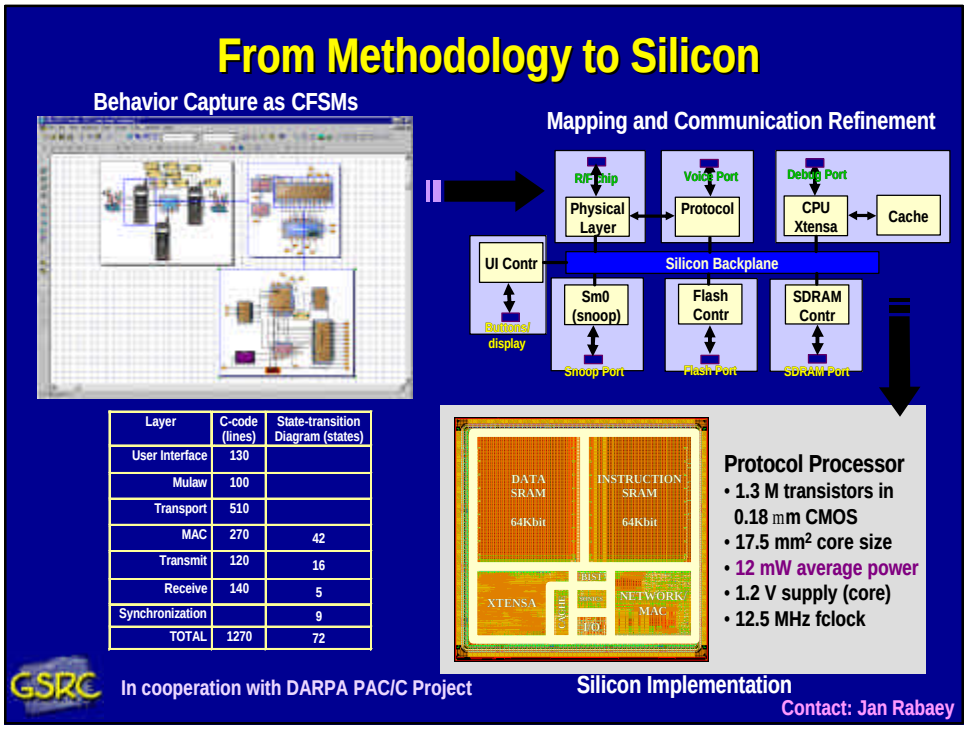
GSRC

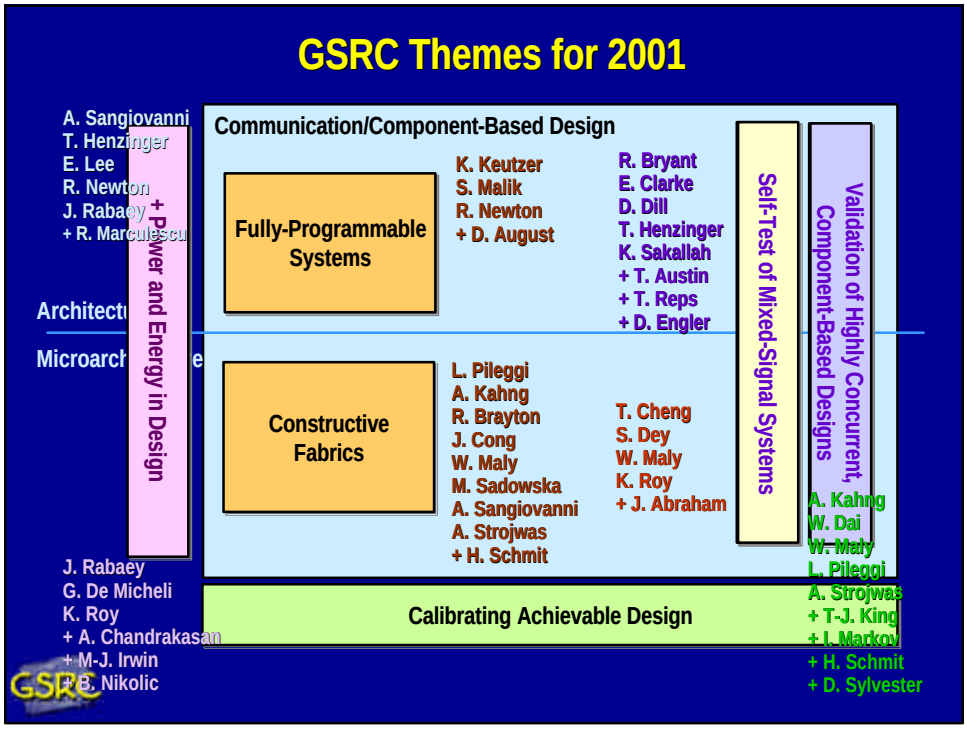
Contact: Larry Pileggi

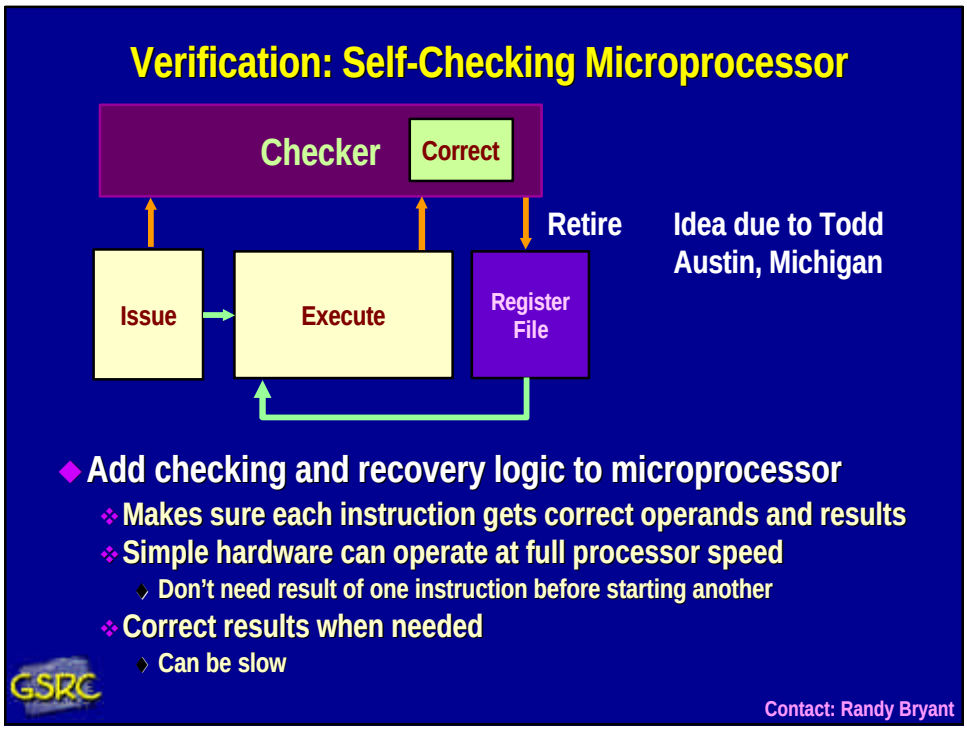


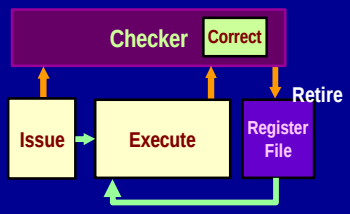




# Benefits of Self-Checking



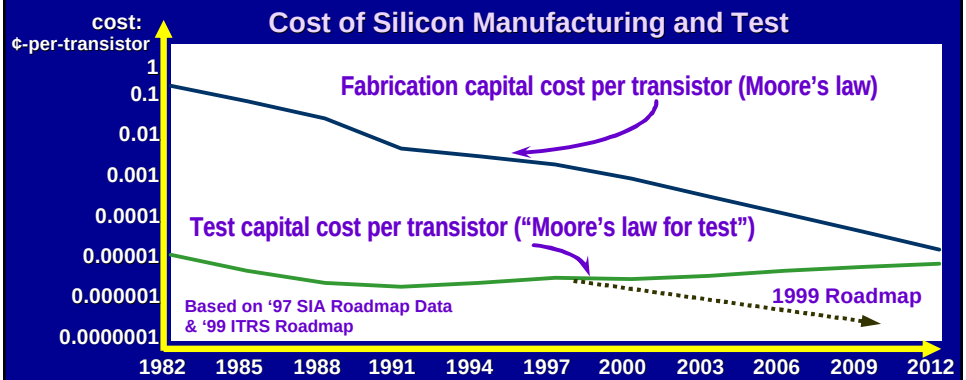

Builds on verification capabilities developed by David Dill (Stanford), Randy Bryant (CMU), and Karem Sakallah (Michigan).

- Validation
  - By verifying the checking/correction logic, we can guarantee correct behavior by overall system
  - Much smaller task than verifying entire system
- Embedded Software
  - Is a critical part of the overall validation problem and will play an increasingly important role in our research. We will most likely tackle it in the context of a family of platforms.
- Reliability
  - Reduced sensitivity to transient effects such as radiation events

GSRC

Contact: Randy Bryant

# New Test Paradigm: Embedded SW-Based Self-Testing & Mixed-Signal BIST




Test paradigms:

- Functional testing (manual TG)
- Structural testing (scan, ATPG)
- Built-in self-test (embedded HW tester)
- Embedded SW-based self-test (embedded SW tester)
- Analog/Mixed-signal DfT/BIST

GSRC

Contact: Tim Cheng

## Research Agenda–GSRC Test Theme

- Embedded Software-Based Self Testing
  - Platforms and methods for systematic design of embedded software (SW) self-tester
  - System-level DfT techniques to support SW-based self-test
  - Embedded SW-based self-diagnosis
  - Embedded SW-based defect characterization
- Analog/Mixed-Signal Self-Testing
  - DSP-based self-testing of analog/mixed-signal components
  - Self-testing of high-resolution ($\Sigma\Delta$ 16 bits) converters
  - On-chip measurement for high-speed serial communication links

GSRC

Contact: Tim Cheng

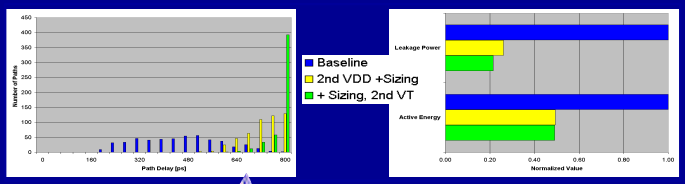
## "Power and Energy in Design" – Vision
### (Joint with Interconnect FCRP)

We are developing platform architectures that combine static and dynamic techniques to select the operational parameters (voltage, frequency, threshold), minimizing energy or power dissipation (active and standby) while meeting performance constraints

GSRC

Contact: Jan Rabaey

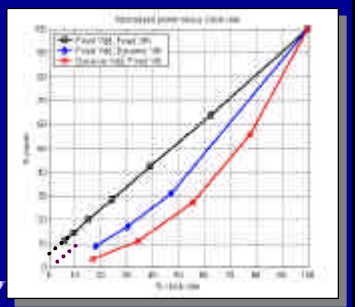
## Classification and Quantification of Power Management Techniques as a Function of Activity (Active + Standby)




Example: Leakage management techniques

Activity 100% → 0% standby

| | | |
|---|---|---|
| Compile Time | Logic Styles, Stacked Transistors, Transistor Sizing Multiple Vdd Multiple Vt | |
| Run Time | Dynamic Vdd (DVS) Dynamic Vt (DVTS) | Signal Conditioning Supply resistance Power down DVS, DVTS |



*White Paper under Development*

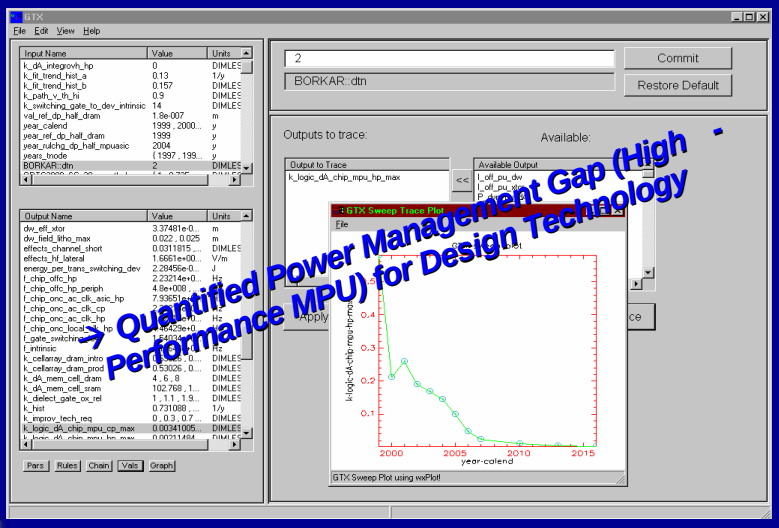
Contact: Jan Rabaey

## "Living ITRS-2001" in GTX

- First time ever: consistency checks, unified assumptions for power, frequency, die size, density, performance
- Creates linkages between Design, Assembly/Packaging, Defect Reduction, Process Integration / Devices / Structures, Test, Overall Roadmap Technology Characteristics, …
- Models and studies are linked with ITRS-2001 distribution
- Improves flexibility, quality, transparency of roadmapping
  - Allows semiconductor industry to better allocate R&D investment: "Who should solve a given red brick wall?"
- 2002 goal: Increase fraction of ITRS captured within GTX

Contact: Andrew Kahng

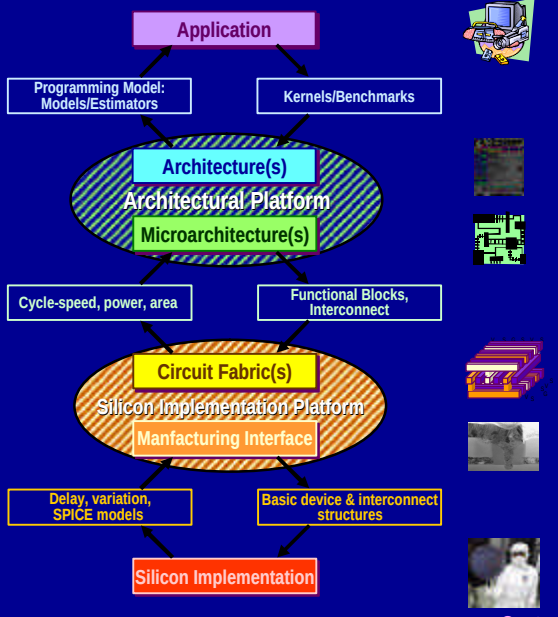
## "Living ITRS" Example Study: Maximum Chip Area Containing High-Performance Logic (PIDS Chapter), Subject to Power Limits (Assembly/Packaging Chapter)



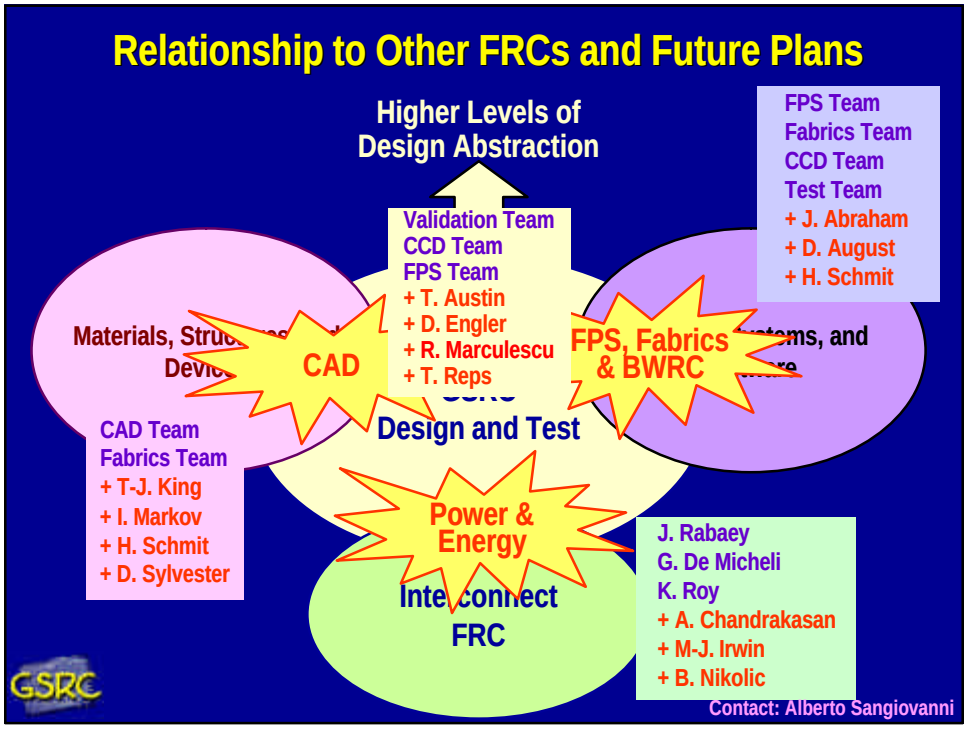

→ Quantified Power Management Gap (High-Performance MPU) for Design Technology

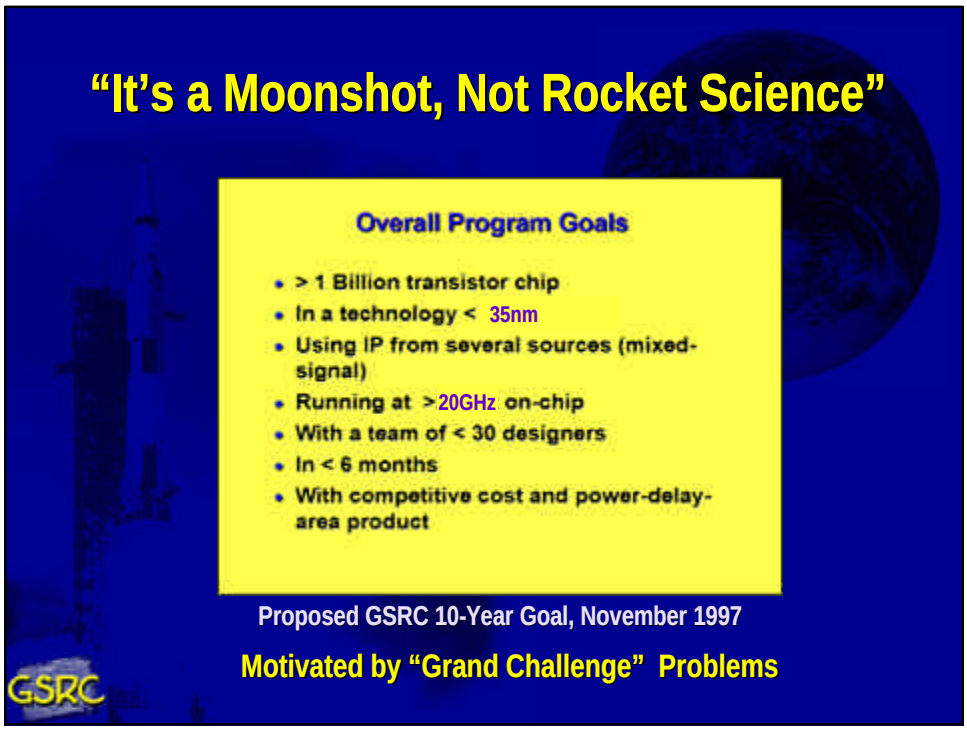
Contact: Andrew Kahng

## A Discipline of Platform-Based Design




Contact: Alberto Sangiovanni



## "Not Just Research As Usual"

- The GSRC is a unique experiment in long-range, collaborative research, enabling broad collaboration across many areas of EDA and Design
- In the 1960-1980's DARPA played a key role in creating and maintaining a collaborative community in design and architecture
  - Xerox PARC & the Alto, Berkeley Unix, RISC, RAID, Integrated EDA Systems…
- GSRC is about rebuilding and maintaining such a community of researchers in many fields related to design productivity
  - By leveraging modern, distributed collaborative infrastructure
  - By enabling and supporting a series of research themes
  - By developing and maintaining a well-defined, but broad goal—the Moon Shot—that serves to integrate all participants

GSRC

Contact: GSRC Team!