

# INVENTRA™

THE INTELLIGENT APPROACH TO INTELLECTUAL PROPERTY

## Viterbi ENCODER/DECODER

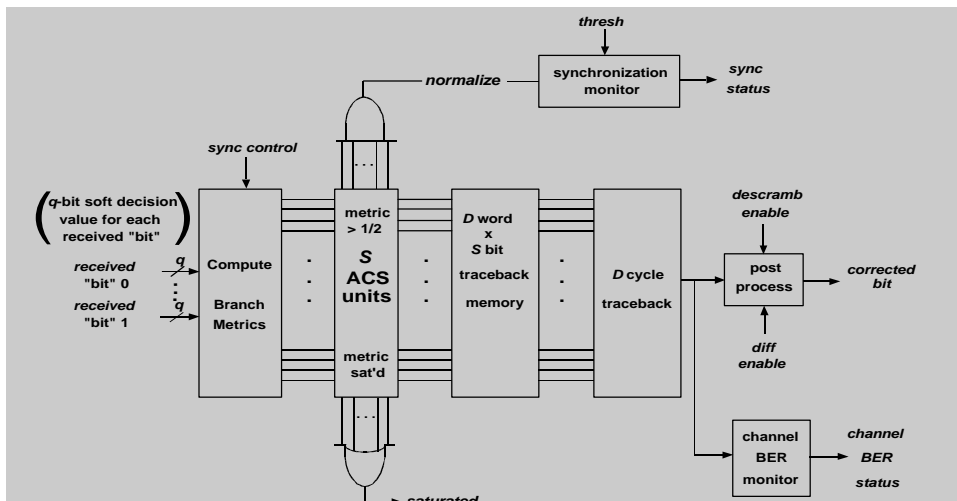
### FUNCTION

Performs a real-time, fixed latency, maximal-likelihood detection of 1-bit information encoded with an  $n$ -bit convolutional code. Constraint length, chain-back depth, encoder generating functions, and code-, soft decision-, and accumulated state metric- wordlengths are parameterized and can be set to meet design specifications. Code words are input in parallel at the information symbol rate. Code bits can be soft decisions of arbitrary wordlength ( $q$ ). The decoded information data stream is output at the information symbol rate. State metrics are normalized whenever all metrics exceed half of their range; the metric Normalization rate can be monitored by observing the normalize output signal. Saturating arithmetic guarantees against state metric overflow. A full state-parallel implementation is available for very high speed applications while a resource-shared implementation is available for area-efficient implementations. Synchronization status, de-scrambling, differential decoding, and channel bit-error-rate monitoring operations are also included. A convolutional encoder is also available.

### PARAMETER DESCRIPTION

- ◆ **acs\_mem\_type:** ACS unit memory type (resource-shared)
- ◆ **ber\_insync\_en:** Determines if bit error rate and sync monitor options are incorporated
- ◆ **D:** Chain-back depth; number of branches in traced-back paths
- ◆ **g0-g4:** Encoder functions (in octal) associated with received code
- ◆ **L:** Constraint length; length of encoder shift register; number of trellis states is given by  $2^{(L-1)}$
- ◆ **n:** Code wordlength; number of code bits;  $1/\text{code rate}$
- ◆ **number\_of\_PEs:** Number of ACS processing elements (resource-shared)
- ◆ **q:** Soft decision wordlength for each code bit
- ◆ **swidth:** Accumulated state metric wordlength
- ◆ **symbol\_period:** Total number of symbols to count in the sync monitor
- ◆ **tb\_mem\_type:** Trace-back memory type

### FUNCTIONAL DESCRIPTION



## I / O P O R T S ( D E C O D E R O N L Y )

**received\_code:**  $n$   $q$ -bit received code symbols

**rst:** Synchronous reset coincident with the first valid input symbol

**diff\_enable:** Enables differential decoding

**scramb:** Enables CCITT or IESS scrambling

**threshold:** Normalization rate threshold for sync monitor

**clk:** Internal clock (if resource-shared)

**sclk:** Symbol clock

**sync\_out:** Pulses high coincident with the first valid output sample following a reset

**decoded\_data:** Decoded output data stream (1-bit)

**normalize:** Output signal which equals '1' whenever the state metrics are normalized

**saturated:** Output signal which equals '1' whenever any accumulated state metric has saturated

**insync:** Active low signal signifies an out of sync condition

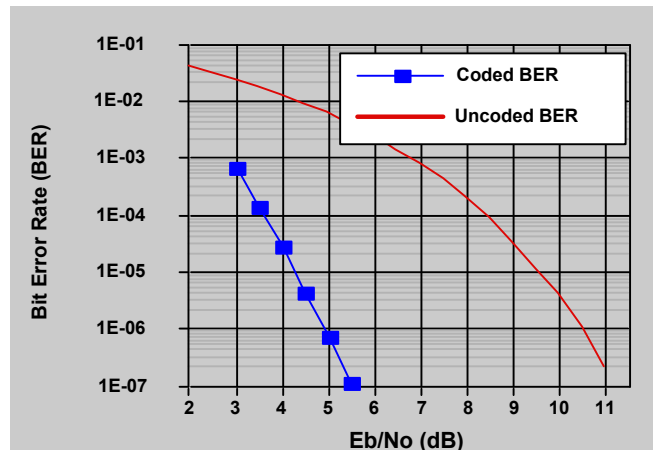
**bercnt:** Measured channel bit error rate

**berclr:** Latches in bercnt and clears ber counter

## E X A M P L E C O D I N G P E R F O R M A N C E

### SPECIFICATIONS:

- Constraint length 7, rate 1/2 encoder/decoder
- 48 state chainback depth
- 3-bit soft-decision decoder inputs

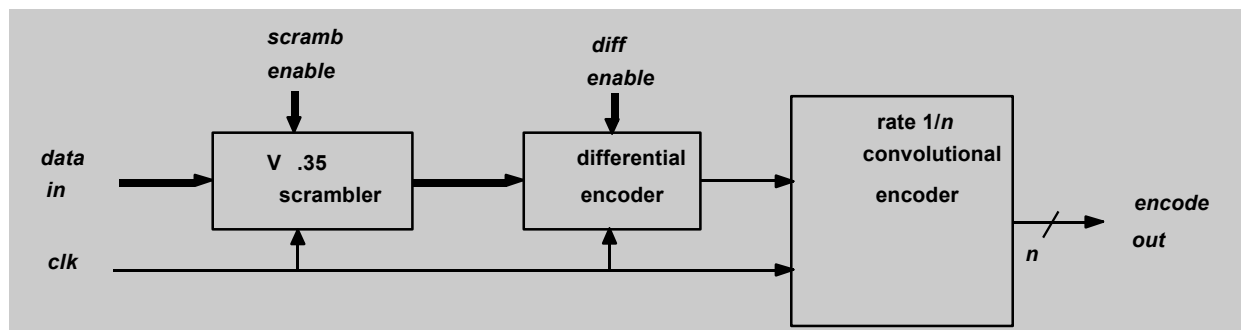


## E X A M P L E P E R F O R M A N C E ( S e e a b o v e s p e c i f i c a t i o n s )

Viterbi Decoder Synthesized to a 0.5  $\mu$ m CMOS Process, *nominal conditions*

	Area Optimized	Speed-Area Balanced	Speed Optimized
# ACS Units	1	8	64
Speed (Msps)	0.810	6.32	85
Gates	3,200	19,400	34,900

## F U N C T I O N A L D E S C R I P T I O N ( E N C O D E R )



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