Summary of Homework 2

Component IP Blocks

David Chinnery

Application Specific Components

Marlene Wan and Ning Zhang

Component	Description	Cost	Area	Power	Use Model	Comments
4i2i Reed-Solomon	CODEC	once off/ per unit	7k to 17k gates		C and C++ software, VHDL and Verilog RTL	700 cycles per codeword (t=3, 12Mbps software), to 6000 cycles per codeword (t=16, 1.17Mbps software)
Mentor Reed-Solomon	encoder		3k to 6k gates		soft core	78 Msps to 94 Msps in 0.5um, with increasing programmability (t=8)
Mentor Reed-Solomon	real time decoder		9k (t=4), 18k (t=8)		soft core	speed about 45MHz in 0.5um
Mentor	QAM/QPSK modulator				soft core	up to 7 Msps data rate, 100 Msps output sample rate, meets standards
Mentor	QAM demodulator				soft core	up to 10 Msps data rate, input rate up to 40 Msps, meets standards
Mentor, 4i2i FFT	FFT and IFFT		19k to 29k		soft core	512 to 2048 points, period from 40us to 440us
Mentor, 4i2i DCT	DCT and IDCT	once off/ per unit	20k to 33k		soft core	45MHz to 160MHz speed
Mentor, Inicore UTOPIA	ATM interface		10k		VHDL RTL	25, 33 or 50 MHz
Simple Silicon	USB Analog Transceiver		1.2mm^2		GDSII layout and schematic netlist	0.8um CMOS

DES Encryption Components

Michael Shillman

Component	Description	Cost	Area	Power	Use Model	Comments
Inventra	DES		4k gates		VHDL RTL	400 Mbps
Memec Xilinx	DES		316 CLBs, 30k gates		VHDL or Verilog for FPGA	100 Mbps to 172 Mbps depending on FPGA
SICAN	DES		3k gates and 2Kbit ROM		VHDL or Verilog RTL	4 Mbps
Java	DES		35.1K		Java	
Portable C	DES		35.1K		Portable C	

DSP Components

Chris Taylor and Paul Husted

Manufacturer	Description	Cost	Area	Power	Use Model	Comments
DSP Group	PineDSPCore	CV			Hard/Soft Core	
	OakDSPCore	CV			Hard/Soft Core	
	TeakDSPCore	CV			HDL Core	
	PalmDSPCore	CV			Soft Core	
AMS	Software prog.	CV			Hard/Soft/Firm Core	
SGS-Thomson	D950	CV			CV Core	
3Soft Corp.	M320C25	CV			HDL Core	
	M320C50	CV			HDL Core	
Clarkspur	CD2400	CV			CV	
Texas Instr.	TMS320C2xLP	$26.40			Hard Core	
	TMS320C3x	$135			Hard Chip	
	TMS320C54x	$5-$75			Soft (IBM fab) Core	
	TMS320C62x	$21-$224			Hard Chip	
	TMS320C67x	$109-$233			Hard Chip	
Analog Dvcs.	ADSP-2100	CV			Soft Core	
	ADSP-218x	CV			Soft Core	
	ADSP-21020	$159			Hard Chip	
	ADSP-2106x	$64-$358			Hard Chip	
Lucent	DSP32xx	$75			Hard Chip	
Motorola	DSP56800	$52.5-$56			CV Core	
	DSP5600				CV Core	
	DSP96002				CV Chip	
	DSP566xx	$20			CV Chip	
	DSP56300	(Qty. 10000)			CV Core	

Ethernet Components

David Chinnery and one datapoint from Rhett

Component	Description	Cost	Area	Power	Use Model	Comments
Xilinx and CoreEL FPGA	10/100 Mbit/s	$12,500	71K gates, 932 CLBs.	25W on XC4005 FPGA	VHDL for FPGA	25 MHz clock.
Inventra 10100ETH	10/100 Mbit/s		60K gates		soft core	PCI, 2.5 MHz or 25MHz clock
Inventra MAC	10/100 Mbit/s		17K gates			
Inventra GEM-PAK-STD	Gigabit MAC		10K gates		VHDL RTL	Synthesized for 0.5um, 125MHz clock.
CoreEl	Gigabit Ethernet MAC		14.5K gates		VHDL RTL	Synthesized for 0.35um and 0.5um CMOS, max. clock of 133MHz.
LSI Logic E-110	10/100 Mbit/s				Verilog, VHDL source	2.5 MHz or 25 MHz clock, 98% fault coverage in test bed
YAGO Systems MSR Family	Multilayer switching router 10/100 ports, also gigabit ports	$595/port			router in chassis	125MHz clock, ASIC with MIPS VR5000 microprocessor. 0.35um process.
LANCore LC-GMC1000	Gigabit MAC	once off	25K gates RTL, 40K gates on FPGA.	36W on ORCA FPGA	Verilog, VHDL RTL	Optimised for 0.35um CMOS, 3.3V or 5V operation, and ORCA 3C FPGA. 66MHz interface.
Mysticom	Ethernet PHY				GDSII for hard, netlist and SDF for soft	3.3V, 0.35um

Microcontroller Components

Phillip Chong

Component	Description	Cost	Area	Power	Use Model	Comments
Motorola 68HC11	flexible microcontroller	$10		0.135W at 5V	chip	3 MHz, 0.19 MIPS
Motorola Coldfire	32 bit RISC CPU	$25 to $45		0.95W at 90MHz	chip	13.5 to 70 MIPS (at 90MHz), from 0.8um to 0.35um
Hitchi SH-2	32 bit RISC CPU	$45		0.8W	chip	28 MHz, mostly single cycle instructions

PCI Bus Components

Niraj Shah

Component	Description	Cost	Area	Power	Use Model	Comments
Sand Micro.	PCI		10k gates		VHDL or Verilog RTL and for FPGA	32 bit or 64 bit buses for PCI, master FIFO, slave FIFO. Doesn't operate at 66 MHz. 132 Mb/s burst transfer rates.
LSI Logic FlexCore	PCI-66				hard macro	32 bit or 64 bit interfaces, 33 MHz or 66 MHz, up to 100 MHz asynchronous. Built in testability, 99% fault coverage. 1.8V, 2.5V and 3.3V technologies. 0.25um and 0.18um.
Synopsys Design Ware DWPCI	macrocell				VHDL or Verilog RTL	good software support and configurability, 0-33 MHz and 66MHz clock frequencies, 264 Mb/s and 528 Mb/s burst transfer rates respectively.
Lucent	PCI local bus macrocell		8k gates		gate level netlist macro	32 bit or 64 bit buses for PCI, master FIFO, slave FIFO. Doesn't operate at 66 MHz. 132 Mb/s burst transfer rates.
ASIC Designers	PCI				VHDL or Verilog RTL, or gate level netlist macro	32 bit and 64 bit PCI bus widths, speeds up to 66 MHz, host bus up to 100 MHz.

Viterbi Components

Scott Weber with datapoints from Marlene and Ning, and Rhett

Component	Description	Cost	Area	Power	Use Model	Data Rate
Inventra ts_viterbi_59		$92,160	12k gates		Soft Core	1.51 MHz
Inventra viterbi_36		$92,160	80k gates		Soft Core	12.3 MHz
Alantro Viterbi		$40,000	26k gates		Soft Core	25 Mbs
Alantro Trellis		$40,000	26k gates		Soft Core	75 Mbs
SPA on ADSP_218x		$55,000 $35,000 $10,000	Code bits 100800 Data bits 121600		Software	38000 bps
Hantro on Altera EPF10K10			500/576 LCs	7.6W	Soft RTL FPGA netlist	2.8 Mbs
CAST on Xilinx Virtex		XNF $17,500 RTL $32,000	241 CLBs		Soft RTL FPGA netlist	3.75 Mbs

Conclusions

- Most components came with a range of options
- Area varies widely depending on speed (parallelism) and options
- Power estimates unavailable (customer implementation specific)
- Where there are standards the components conform
- Most vendors prefer to discuss price with customer
- Price depends on competition - Viterbi expensive, Ethernet cheaper
- Developing industry, some components in test stage

DSPs

	Family	Delivery	Core or Chip	Feature Size	Arithmetic	Data Width (bits)	(MIPS or MFLops)	Voltage	Cost(Qty. 1,000)	Applications
	PineDSPCore	Hard/Soft	Core	0.6u	fixed	16	40	3.3,5.0	CV	Multimedia appl
DSP Group	OakDSPCore	Hard/Soft	Core	0.5u	fixed	16	40	3.3,5.0	CV	
	TeakDSPCore	HDL	Core	0.25u	fixed	16	260	3.3,5.0	CV	Multimedia appl.
	PalmDSPCore	Soft	Core	0.18u	fixed	16-24	560	down to	CV	Telecommunications
AMS	Software prog.	Hard/Soft/Firm	Core	CV	fixed	16	50	3.3	CV	Telecommunications
SGS-Thomson	D950	CV	Core	CV	fixed	16	40	3.3	CV	Multimedia, telecom appl.
	M320C25	HDL	Core	CV	fixed	16	15	3.3,5.0	CV	ASIC implementation
3Soft Corp.	M320C50	HDL	Core	CV	fixed	16		5	CV	
Clarkspur	CD2400	CV		CV	fixed	16	25		CV	Fax Modem
	TMS320C2xLP	Hard	Core	0.35u	fixed	16	40	5	$26.40	
Texas Instr.	TMS320C3x	Hard	Chip	.18u	floating	32	20-30	3.3,5.0	$135	TI ASIC Fab will incorporate any DSP core into design for volumes worth minimum $5 million / year
	TMS320C54x	Soft (IBM fab)	Core	0.25-0.18u	fixed	16	100-200	1.8,2.5	$5-$75	
	TMS320C62x	Hard	Chip	.18u	fixed	16	1200-2000	1.8,3.3	$21-$224	
	TMS320C67x	Hard	Chip	.18u	floating	32	1000	1.8,3.3	$109-$233	
Analog Dvcs.	ADSP-2100	Soft	Core	0.6,0.5	fixed	16	40	3.3,5.0	CV	SignalProcessing
	ADSP-218x	Soft	Core	0.5,0.45,0.35	fixed	16	33	3.3,5.0	CV	
	ADSP-21020	Hard	Chip		floating	32	33	5	$159	Imaging,Milt. appl.
	ADSP-2106x	Hard	Chip	0.5,0.45,03.5	floating	32	40	3.3,5.0	$64-$358	
Lucent	DSP32xx	Hard	Chip	CV	floating	32	20	5	$75	Multimedia appl.
Motorola	DSP56800	CV	Core	0.35	fixed	16	20	3.3	$52.5-$56	Wireless appl.
	DSP5600	CV	Core	0.65,0.55	fixed	24	80-100	3.3		Cellular appl.
	DSP96002	CV	Chip		floating	32	20			Only floating pt.
	DSP566xx	CV	Chip	0.35	fixed	16/24	16	1.8	$20(Qty. 10,000)	
	DSP56300	CV	Core	0.5,0.42,0.36	fixed	24	66/80/100	3		Telephony

Viterbi Summary

name	k/n	L	q	D	ACS	Data Rate	Gate Count	Cost	Use Model
Inventra ts_viterbi_59	½	7	3	96	1	1.509 MHz	12034	$92,160	Soft Core
Inventra viterbi_36	½	7	3	96	6	12.3 MHz	80308	$92,160	Soft Core
Alantro Viterbi	1/3, ½, 2/3, ¾, 7/8	7	3	96	???	25 Mbs	26,000	$40,000	Soft Core
Alantro Trellis	1/3, ½, 2/3, ¾, 7/8	7	3	96	???	75 Mbs	26,000	$40,000	Soft Core
SPA on ADSP_218x	½, ¾, 7/8, 1/3	7	Hard	???	1	38000 bps	Code: 100800 bits Data: 121600 bits	$55,000 $35,000 $10,000	Software
Hantro on Altera EPF10K10	½	7	3	55	4	2.8 Mbs	500/576 LCs	???	Soft RTL FPGA netlist
CAST on Xilinx Virtex	½	7	3	55	4	3.75 Mbs	241 CLBs	XNF $17,500 RTL $32,000	Soft RTL FPGA netlist