Viterbi IP

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Component Based Design

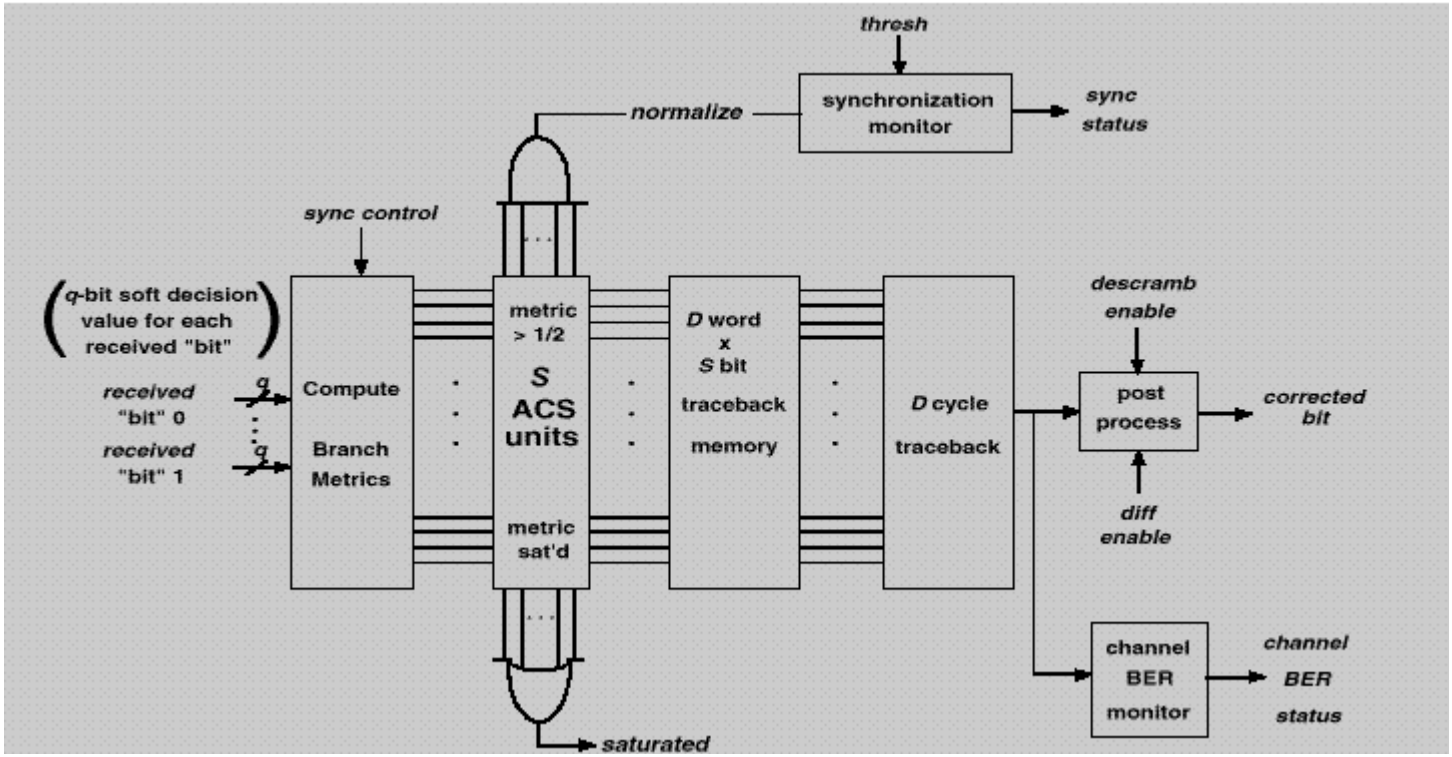
Inventra Viterbi IP

- Parameterized Viterbi encoder/decoder
- Resource-shared (area-efficient)
- Full state-parallel (high speed)
- Available also
  - Synchronization status
  - De-scrambling
  - Differential decoding
  - Channel bit-error-rate monitoring
  - Convolutional encoder
- Soft configurable IP (RTL HDL)

Inventra Viterbi Parameters

- Parameters
  - Constraint Length (L)
  - Chain-back depth (D)
  - Encoder generator functions (g0-g4)
  - Code length (n)
  - Soft decision wordlength (q)
  - Accumulated state metric wordlength (swidth)

Inventra Viterbi IP



Inventra Configurations

- http://www.mentor.com/inventra/index.html
- Explore a whole range of parameters
- Full state-parallel implementations for high performance
  - Clock Rate from 103.133 MHz to 131.194 MHz
  - Gate Counts from 7175 to 459522
  - Price Ranges from $60,000 to $92,160
- Resource-shared implementations for area efficiency
  - Clock Rate from 65.432 MHz to 97.417 MHz
  - Data Rate from 0.255 Mbs to 20.935 Mbs
  - Gate Counts from 4485 to 211161
  - Price Ranges from $60,000 to $92,160

Alantro Viterbi IP

- 64 state Viterbi Encoder/Decoder
- Optimized for power/space minimization
- Fully synchronous
- Design customizations
  - Multiple Rates : 1/3, 1/2, 2/3, 3/4, 7/8 or fully programmable using external logic
  - BPSK and QPSK using Viterbi Mode
  - 8-PSK and 16-PSK using Trellis Mode
  - 4-bit soft decision or 1-bit hard decision
  - Trace-back depth (hard coded or programmable)

Alantro Numbers

- Approximated at 26,000 gates and 16k bits of single port RAM (96 symbol trace-back depth)
- 25 Mbs in Viterbi mode
- 75 Mbs in Trellis mode
- $40,000 for the core plus a royalty structure based on volume
- Verilog-HDL source, test benches, and test-vectors

SPA Viterbi IP

- Software for ADSP-21xx series DSP (~100 mW, 0.35um)
- >38000 bps on a 66 MIPS processor
- Standard constraint length k = 7
- Rates supported: 1/2, 3/4, 7/8, 1/3
- 13 bit branch metrics, 16 bit state metrics
- Code size: 100800 bits
- Data memory: 121600 bits
- Industry standard FEC algorithms

SPA Viterbi IP

- Source code with unlimited copies: $55,000
- Object code with unlimited copies: $35,000
- $1.50 per copy with an up-front cost of $10,000

Hantro Viterbi IP

- Soft Decision Decoder
- Customize Parameters
  - Soft Decision word length
  - Constraint length (K)
  - ACS cells
  - Length of trace-back
  - Coding rate
  - Coding Polynomial
- Can include BER monitor, change in modulation type, and add a microprocessor interface

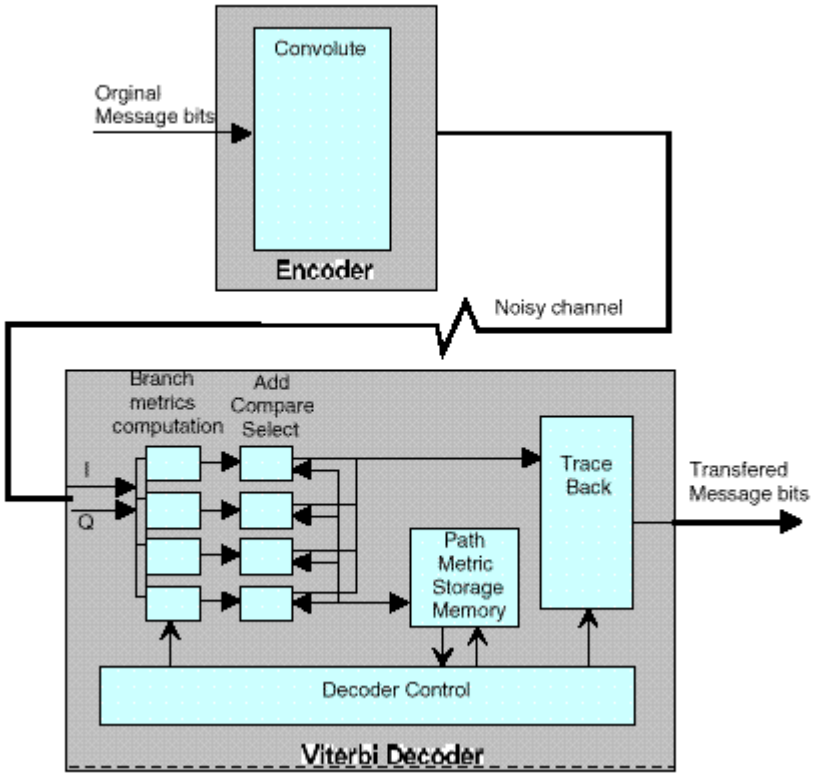
Hantro Viterbi IP

- VHDL RTL source code
- Testbench
- Example testbench wrapper for post-route simulation
- Vectors for testbench
- Simulation script
- Synthesis script
- Expected results for testbench

Hantro Configuration

- Configuration:
  - Coding Rate (R) = 1/2
  - Constraint Length (K) = 7
  - Number of soft input bits = 3
  - Trace-back length = 55
  - Number of ACS elements = 4
- 500/576 LCs on an Altera EPF10K10, 5120 RAM bits
- 0.35μm process
- Clock Rate = 45 MHz
- Power = ~7.6 W
- Data Rate = 2.8125 Mbs

Hantro Viterbi IP



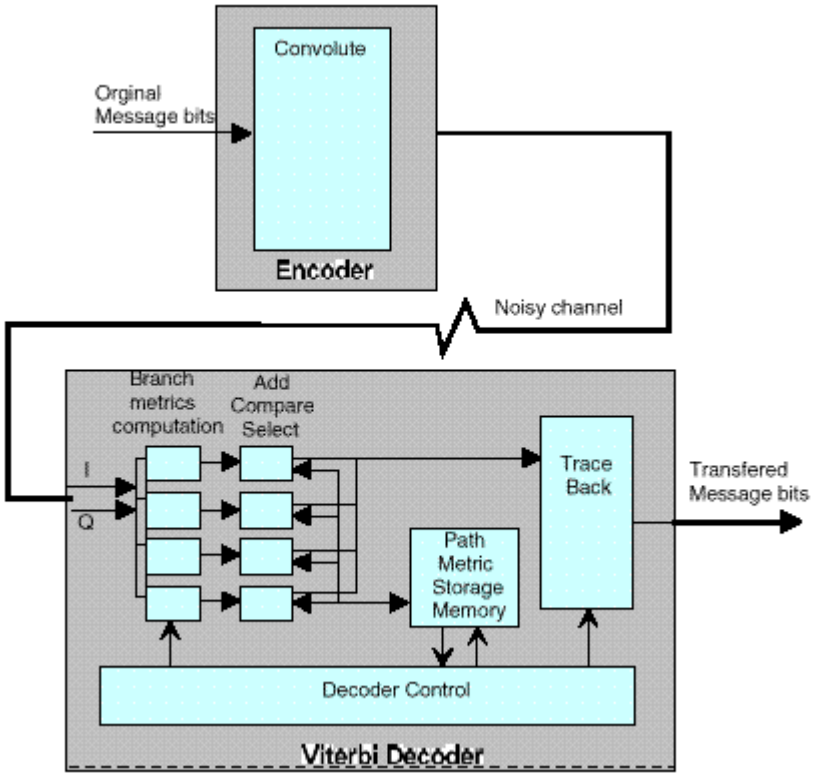
CAST Viterbi IP

- Identical to Hantro's IP
- Configuration:
  - Coding Rate (R) = 1/2
  - Constraint Length (K) = 7
  - Number of soft input bits = 3
  - Trace-back length = 55
  - Number of ACS elements = 4
- 241 CLBs on the Xilinx Virtex
- Data Rate = 3.75 Mbs

CAST Viterbi IP

- One time site license
  - XNF netlist is $17,500
  - RTL source is $32,000
- Support and maintenance for 15% annually
- Delivered with test vectors, test benches, and expected results

CAST Viterbi IP



4i2i Viterbi IP

- C, C++, VHDL, Verilog models
- Configurable parameters like others
- Flexible licensing
  - one-off license payment
  - per-unit license payment
- No performance data points

SICAN Viterbi Decoder

- Soft module
- Performance varies so much the representative stated
- $100,000 license

Summary

name	k/n	L	q	D	ACS	Data Rate	Gate Count	Cost	Use Model
Inventra ts_viterbi_59	½	7	3	96	1	1.509 MHz	12034	$92,160	Soft Core
Inventra viterbi_36	½	7	3	96	6	12.3 MHz	80308	$92,160	Soft Core
Alantro Viterbi	1/3, ½, 2/3, ¾, 7/8	7	3	96	???	25 Mbs	26,000	$40,000	Soft Core
Alantro Trellis	1/3, ½, 2/3, ¾, 7/8	7	3	96	???	75 Mbs	26,000	$40,000	Soft Core
SPA on ADSP_218x	½, ¾, 7/8, 1/3	7	Hard	???	1	38000 bps	Code: 100800 bits Data: 121600 bits	$55,000 $35,000 $10,000	Software
Hantro on Altera EPF10K10	½	7	3	55	4	2.8 Mbs	500/576 LCs	???	Soft RTL FPGA netlist
CAST on Xilinx Virtex	½	7	3	55	4	3.75 Mbs	241 CLBs	XNF $17,500 RTL $32,000	Soft RTL FPGA netlist

Conclusions

- Parameter choice is key to speed/size/power
- Reasonable parameters for hardware/software
- Soft decoder is probably the most important
- Branch metrics have to be finalized