Strong ARM

Philip Chong

Strong ARM (Description)

- SA-1100, 32-bit, 5-stage pipelined RISC.
- 0.35um, 3 metal layers, at 220MHz, 2.5M transistors, 60mm^2 die, 550mW at max freq.
- JPEG: compiled C code, single-threaded.

Strong ARM (Performance)

- Blocks: 640x480 image, 24 bit full color
  - Image Spliter: 307k iters, 4.6M cycles
  - Image Blocker: 14.4k iters, 72k cycles
  - DCT: 14.4k iters, 24.5M cycles
  - Quantize: 921.6k iters, 14.8M cycles
  - Dequantize: handled by InvDCT
  - InvDCT: 14.4k iters, 22.0M cycles
  - Image Unblocker: pointers the same
  - Image Combiner: 307k iters, 3.7M cycles
- Total:
  - 69.6M+14.7M(cache misses)=84.3 cycles
  - 0.35u, 220MHz, 2.6 frames/sec, 0.38 sec/frame
  - 0.25u, 300MHz, 3.6 frames/sec, 0.28 sec/frame

Strong ARM (Power,Cost,Effort)

- Power:
  - double 550mW to get 1.1W
  - 0.42 J/frame
- Cost:
  - RAM: 5M (frame), 8M (total)
  - price: about $22
  - area: 60mm^2(uP)+280mm^2(RAM)=340mm^2
  - 2.3e-10 frames/(lambda^2 s)
- Effort:
  - 1-2 weeks

ARM and ASIC

Ning Zhang & Marlene Wan

ARM+ASIC (Description)

- implementations:
  - pure RISC processor (StrongARM)
  - DCT to configurable ASIC
  - pure ASIC (literature)
  - DSP (literature)

RISC

- Performance: 1.12 sec/frame
- Power: 0.62 J/frame
- Cost: $39
- Effort: 1.5 weeks

RISC+ASIC(DCT)

- Performance: 0.7 sec/frame
- Power: 0.3 J/frame
- Cost: ?
- Effort: 2weeks - 1 month

ASIC (JAGUAR)

- Performance: 10msec/frame
- Power: 0.63mJ/frame
- Cost: 1.5mmx1.7mm in 0.25u
- Effort: 9-28 man-months

DSP (two TIC30's)

- Performance: 2.75s/frame
- Power: ~1W
- Cost: $247.95
- Effort: 1 day compilation

DSP (TMS320C40)

- Performance: 2.6 s/frame
- Power: 3.2 J/frame
- Cost: $160
- Effort: 1day compilation

ASIC

David Chinnery, Rhett Davis

ASIC (Description)

- 3 stage pipeline:
  - 2 1-D DCT:
    - 16 add/sub
    - 22 mult
    - 14 add/mult
  - Quantization
- invDCT use the same pipeline
- claim:
  - Power estimates are accurate to within about a factor of two
  - speed and area estimates are accurate to within about 20%.

ASIC (Performance)

- Assumptions:
  - 0.25 um technology provided by ST
  - 25 MHz clock rate
  - 1.0 V supply voltage
  - Custom multipliers and triple-ported register files
  - Standard cells for the rest (using a library provided by ST)
- Blocks:
  - Mpy: 960ns
  - 1-D DCT: 9600ns
- Total: 0.046s

ASIC (Power, Cost)

- Power:
  - Gated clocks (adds to design time)
  - Supply voltage: 1.0 V
  - Power: 483uW
  - Energy/Frame: 22.2 uJ
  - Minimal static power (100 transistors tied to clock line): 5.3 uW
- Cost:
  - Total chip area: 24.9mm^2

ASIC (Effort)

- Blocks:
  - Specification (3 people, 1 month)
  - Multiplier design (1 person, 3 months)
  - Register file design (1 person, 3 months)
  - Logic/VHDL design (1 person, 1 month)
  - gated clocking system design (1 person, 2 months)
  - component assembly and verification (3 people, 1 month)
- Total: 3 people, ~5 months

DSP

Paul Husted, Chris Taylor

DSP (Description)

- TI’s TMS320C54xx DSP chip
- 16 bit fixed point, .45 mW, or at 120 mW at 200 MIPS
- high-end VC5420:
  - two parallel 100 MIPS DSP cores at 1.8V
- hardware:
  - Three 16-bit data buses and one 16-bit program memory bus
  - 40 bit ACC with 40 bit barrel shifter and two independant accumulators
  - A single cycle non-pipelined MAC
  - Single-instruction repeat and block-repeat operations for program code
  - Block-memory-move instructions for better program and data management
  - Arithmetic instructions with parallel store and parallel load
  - Up to 168K single access RAM Up to 32K dual access RAM
  - Up to 8M word external memory access
  - Six channel DMA controller

DSP (Performance)

- Computation:
  - DCT: 46.1 ms
  - Quantization: 9.22 ms
  - Encoding: 17.8 ms
  - Decoding: 21.6 ms
  - De-quantization: 9.22 ms
  - IDCT: 46.1 ms
  - Total: 149.8 ms/frame
- I/O: 92.2 ms (same time)
- Total: 6.67 frames/sec, 150 ms/frame

DSP (Power, Cost, Effort)

- Power:
  - core CPU: 2.5V, 113mW
  - external pins: 3.0V, 75mW
  - IDLE2(CPU+peripherals): 2.5V, 5mW
  - IDLE3(entirely): 2.5V, 0.013mW
- Cost:
  - Chip: $3 ea.
  - Develop Tools: ~$3k ea.
- Effort: ~3 man-months

Configurable Processor

Niraj Shah
Scott Weber

CP (Description)

- Tensilica's Xtensa configurable uP
- core is a 32-bit RISC, 16 general purpose registers and DSP-like features
- C program, single-threaded
- speeds: 100-250MHz.

CP (Summary)

- Performance:
  - encode: 4 frames/sec, 0.25s /frame
  - decode: 4 frames/sec, 0.25s/frame
- Energy:
  - encode: 31 mJ/frame
  - decode: 32 mJ/frame
  - power: 128 mW
- Cost:
  - encode: 28k bytes (code)
  - decode: 31.6k bytes (code)
  - die: 0.25u, 4.7-5.5 mm^2
- Effort: 100 man-hours

Summary

	RISC (2)	RISC (1)	RISC+ ASIC (2)	ASIC (2)	ASIC (3)	DSP (2)	DSP (2)	DSP (4)	CP (5)
Perf	1.12s	0.28s	0.7s	10ms	46ms	2.8s	2.6s	150ms	250ms
Power	0.62J	0.42J	0.3J	0.63mJ	22.2uJ	1W	3.2J	113mW	128mW 63mJ
Cost	$39	340 mm^2	?	1.5x1.7 mm^2	24.9 mm^2	$248	$160	$3	4.7-5.5 mm^2
Effort	1.5 weeks	1-2 weeks	2weeks 1month	9-28 months	5months	1day	1day	3months	100 hours

Summary

	ASIC	ASIC	DSP	CP	RISC	RISC+ASIC	RISC	DSP	DSP
	N&M	D&R	P&C	S&N	P	N&M	N&M	N&M	N&M
ms/frame	10	46	150	250	280	700	1,120	2,800	2,600
mJ/frame	0.63	0.22	28.50	63	420.00	300.00	620.00	2,800.00	3,200.00
m(s*j)/frame	0.006	0.010	4.3	15.8	118	210	694	7,840	8,320
	1	2	679	2,500	18,667	33,333	110,222	1,244,444	1,320,635