EE290 A: Advanced Topics in CAD
Component Based Design of Electronic Systems
Lecture 5

Professors Kurt Keutzer and Richard Newton

Department of Electrical Engineering and Computer Sciences

University of California at Berkeley

Spring 1999

Outline of issues

Why components?

- Raw silicon capability
- Design productivity

What type of components?

- What size of component?
- What type/capability of component?

How will they be designed?

- Review of implementation alternatives
- Review of common design flows

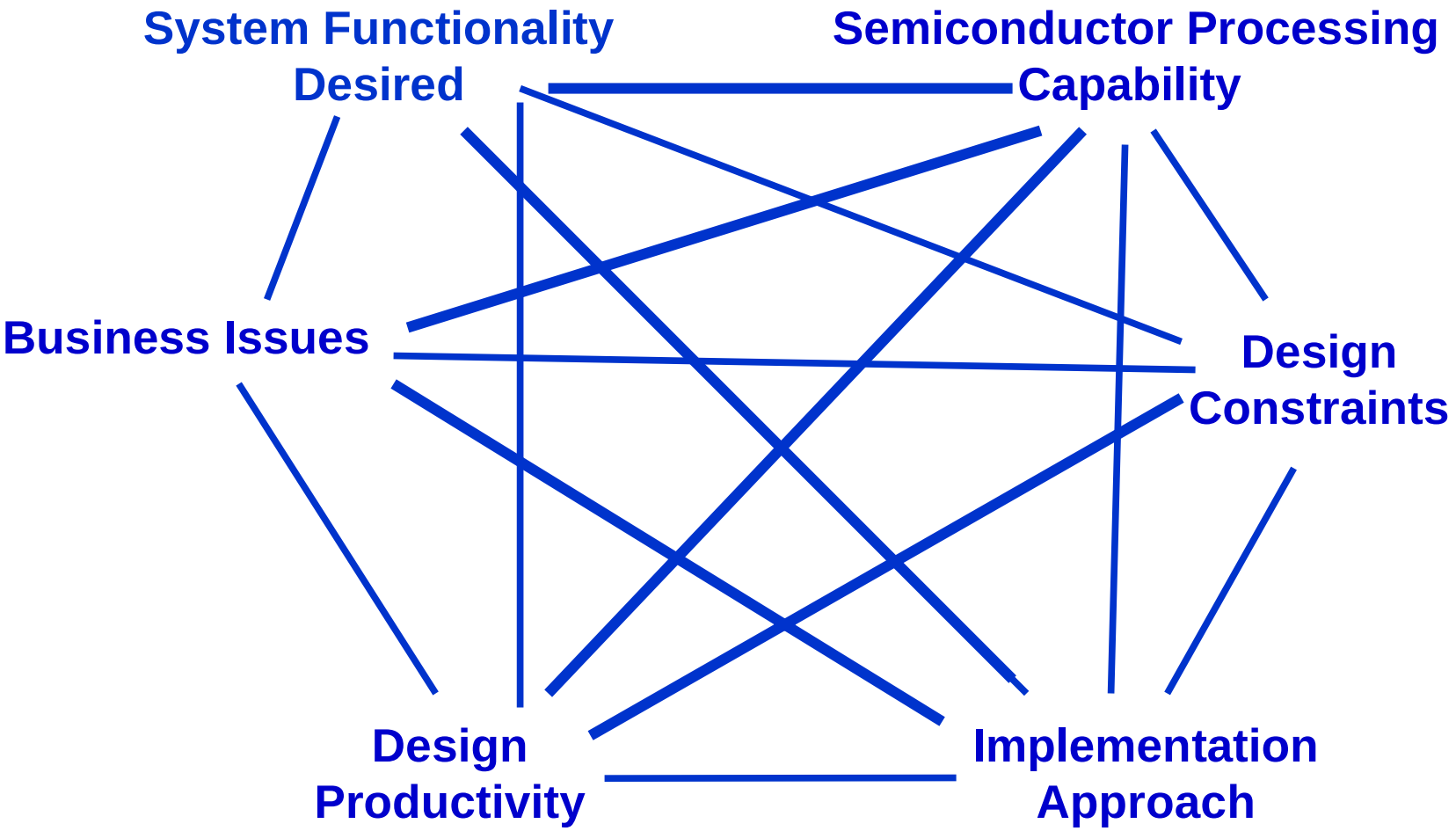
Who are the players?

- foundries,
- fabless semiconductor, 3rd party IP providers, vertical semiconductor,
- system companies

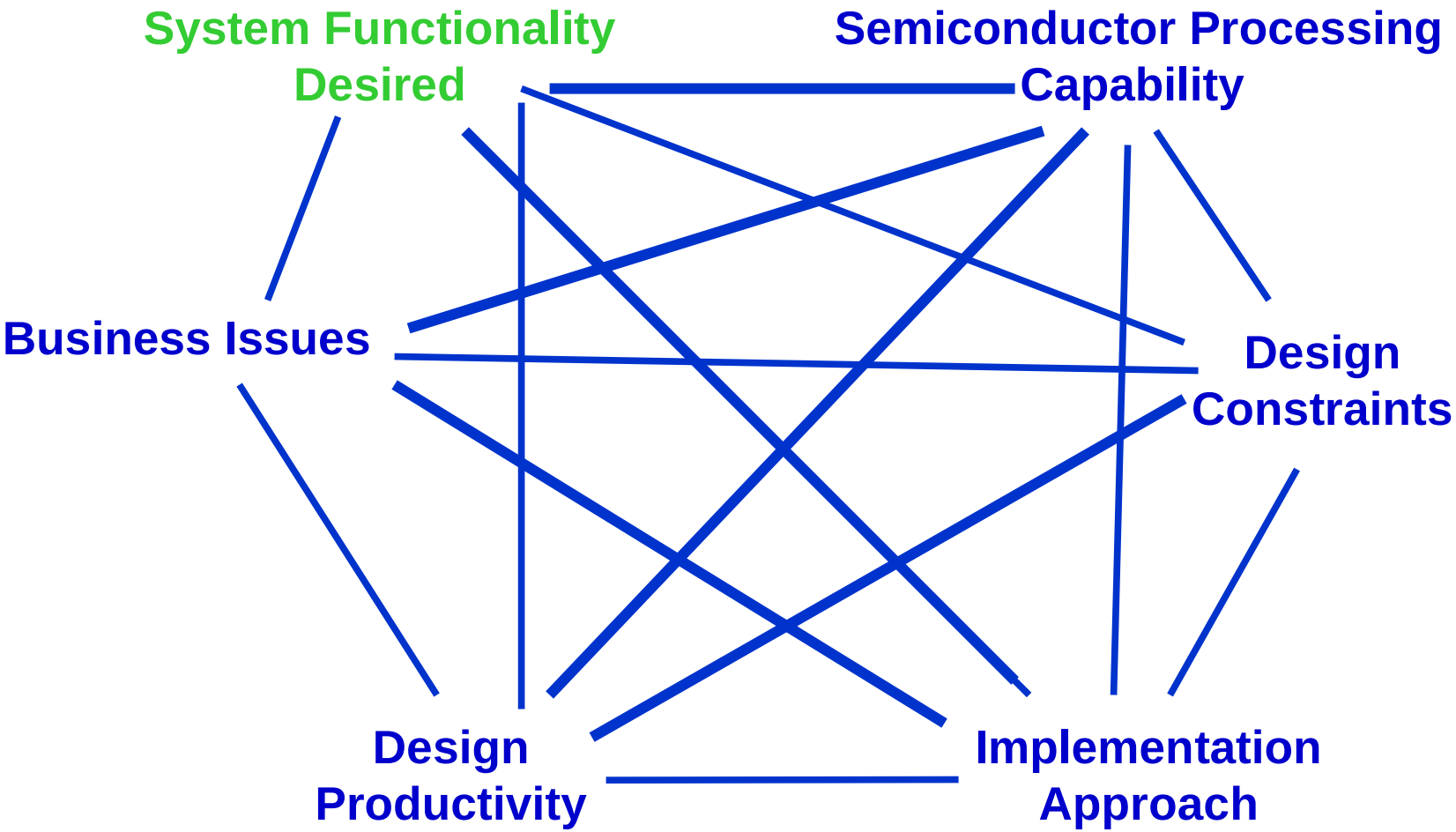
Which design styles are likely to predominate

- Time-to market (productivity)
- Features
  - Process portability
  - In-field up-gradabilty, programmability
  - Quality of results

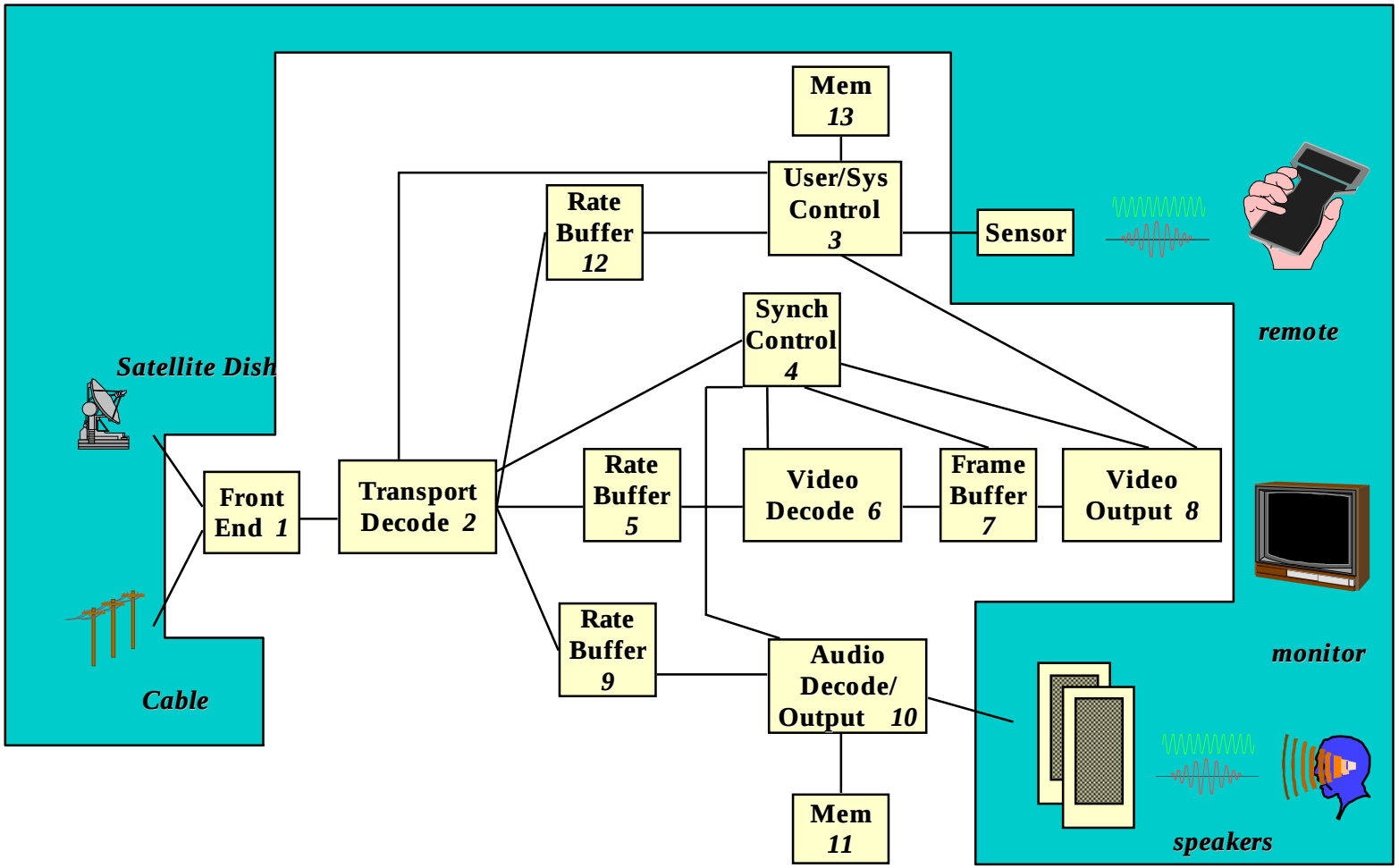
Interrelationship of issues



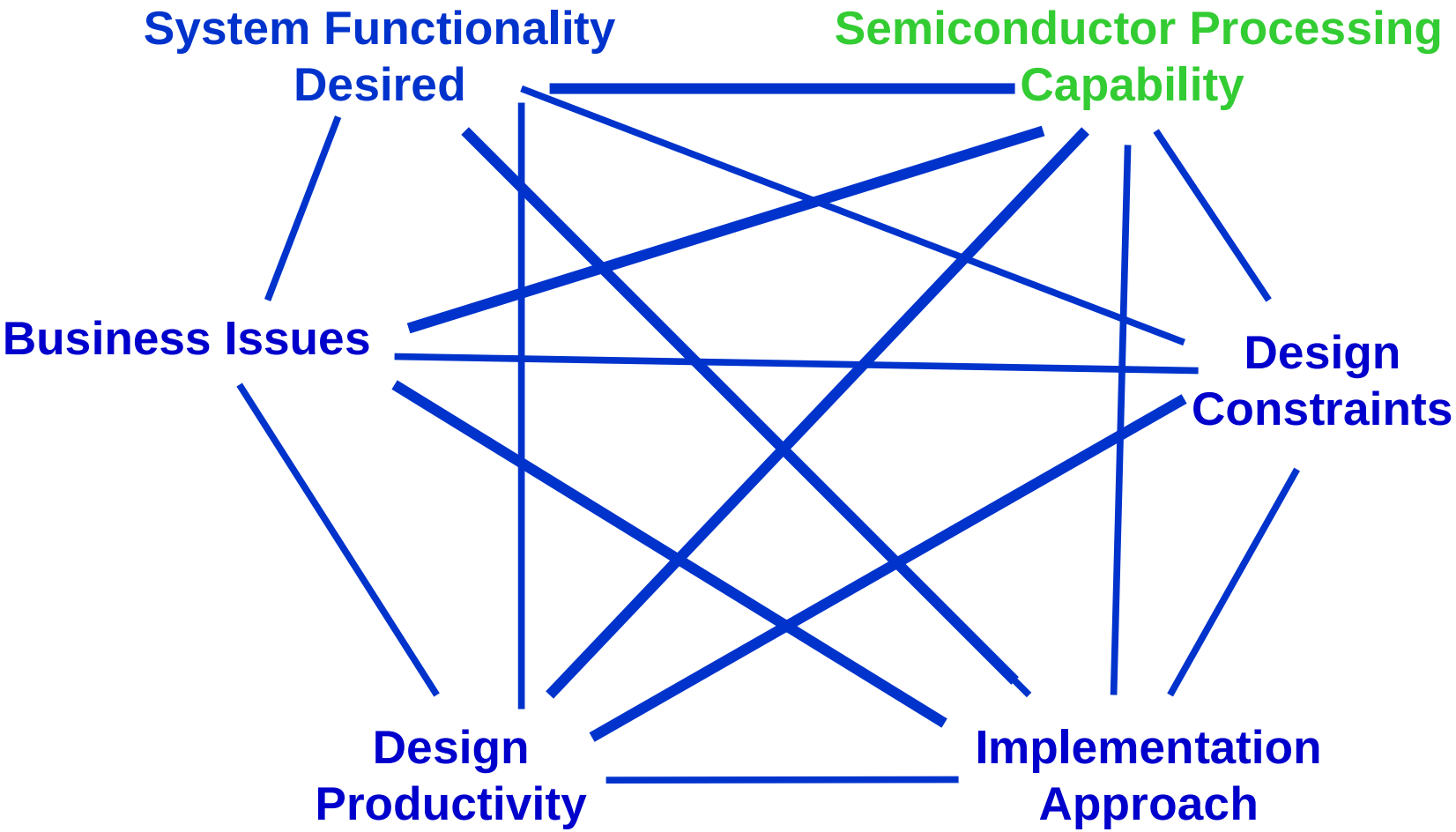
Interrelationship of issues



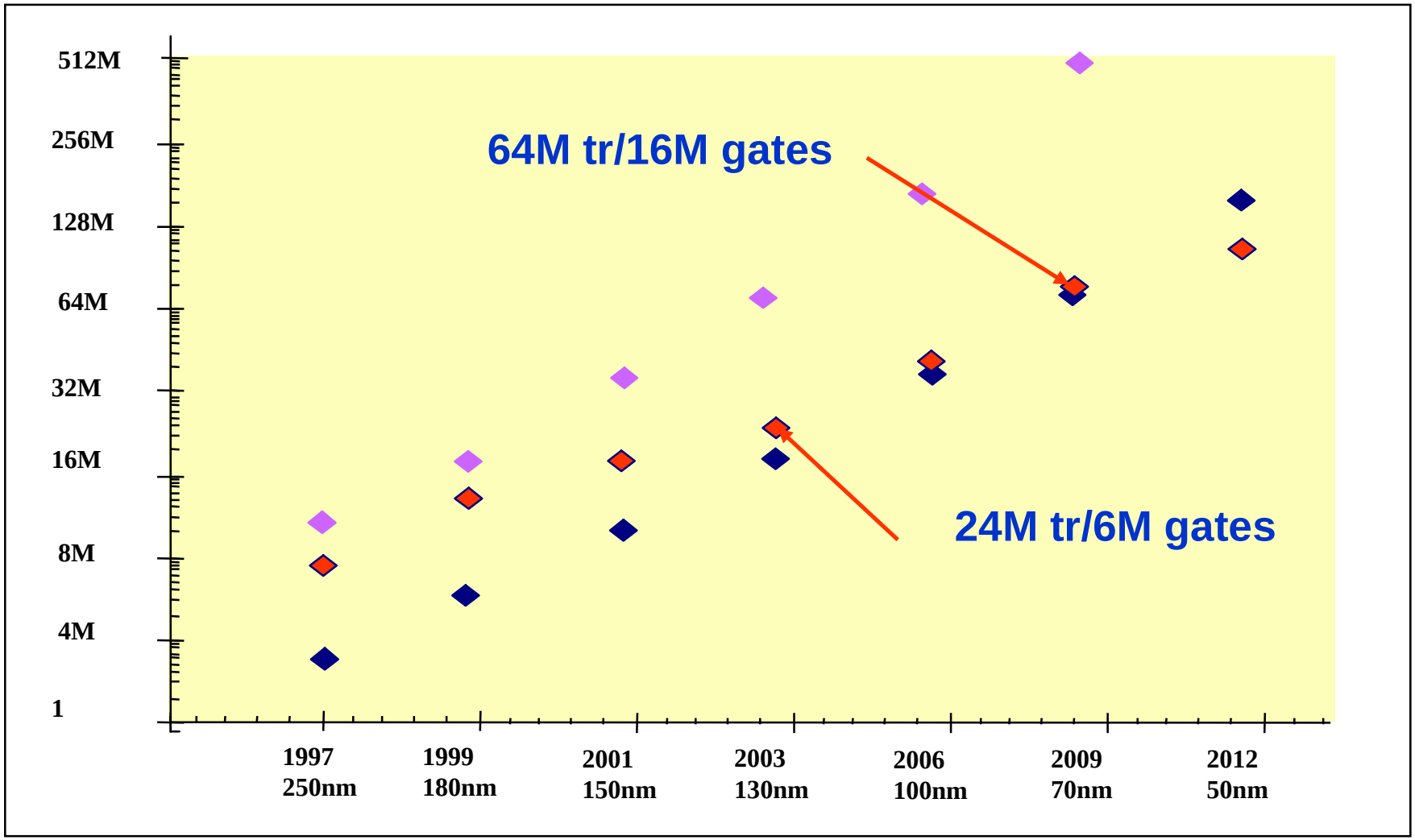
Example of System Behavior - ASVincentelli



Interrelationship of issues

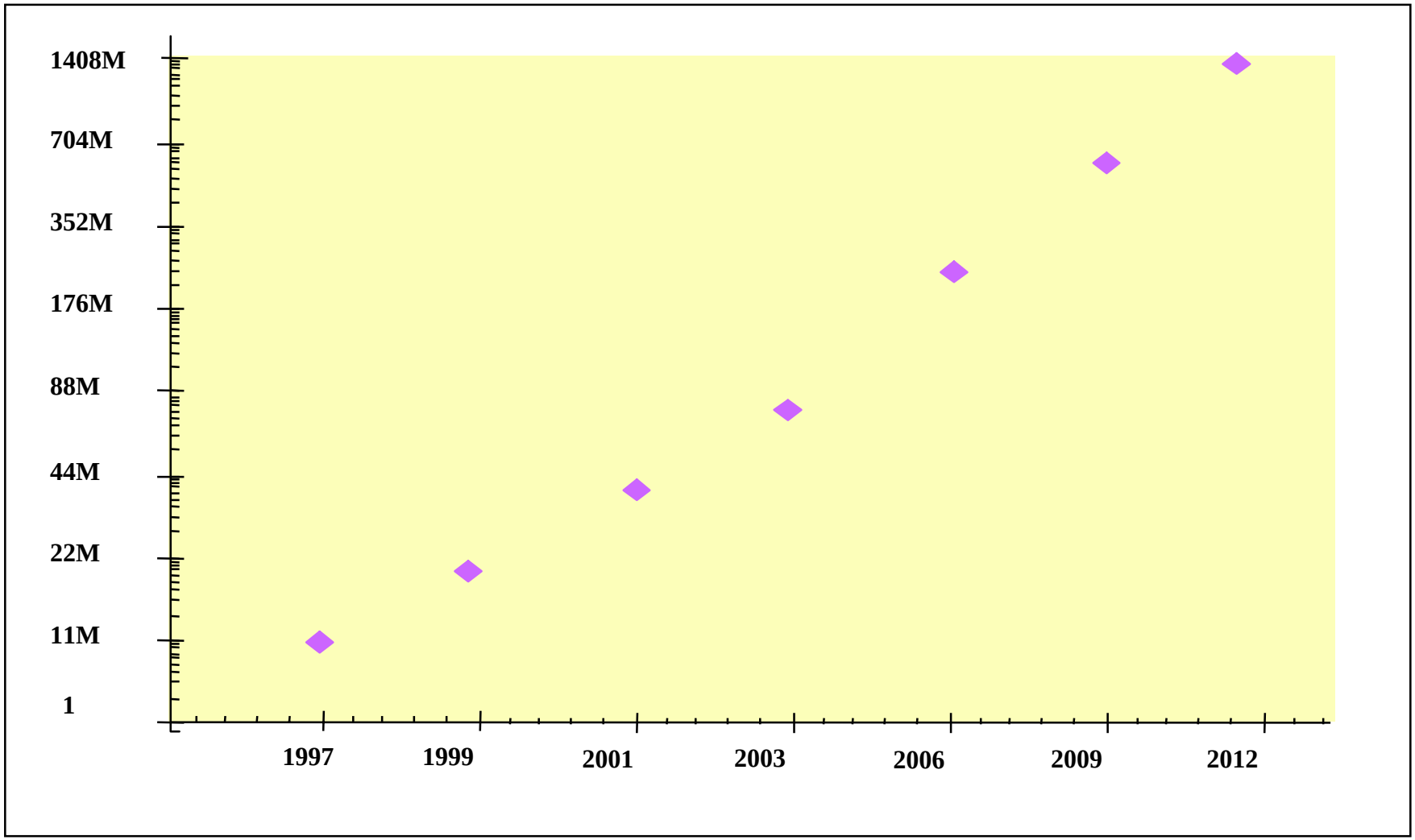


NRTS: Raw Silicon Capability

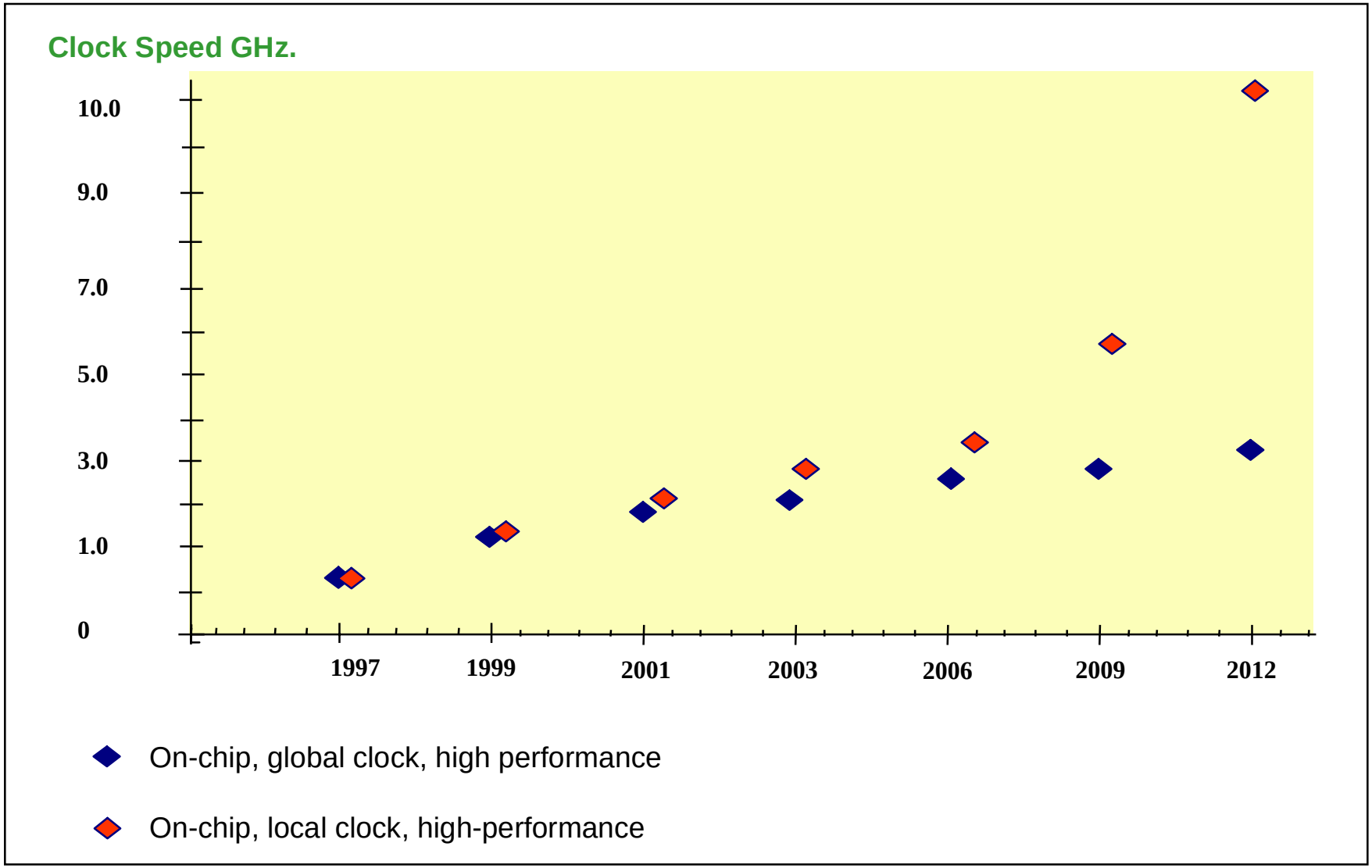


Total microprocessor tr. ◆ Microprocessor logic tr.cm2 ◆ ASIC logic tr. cm2 ◆

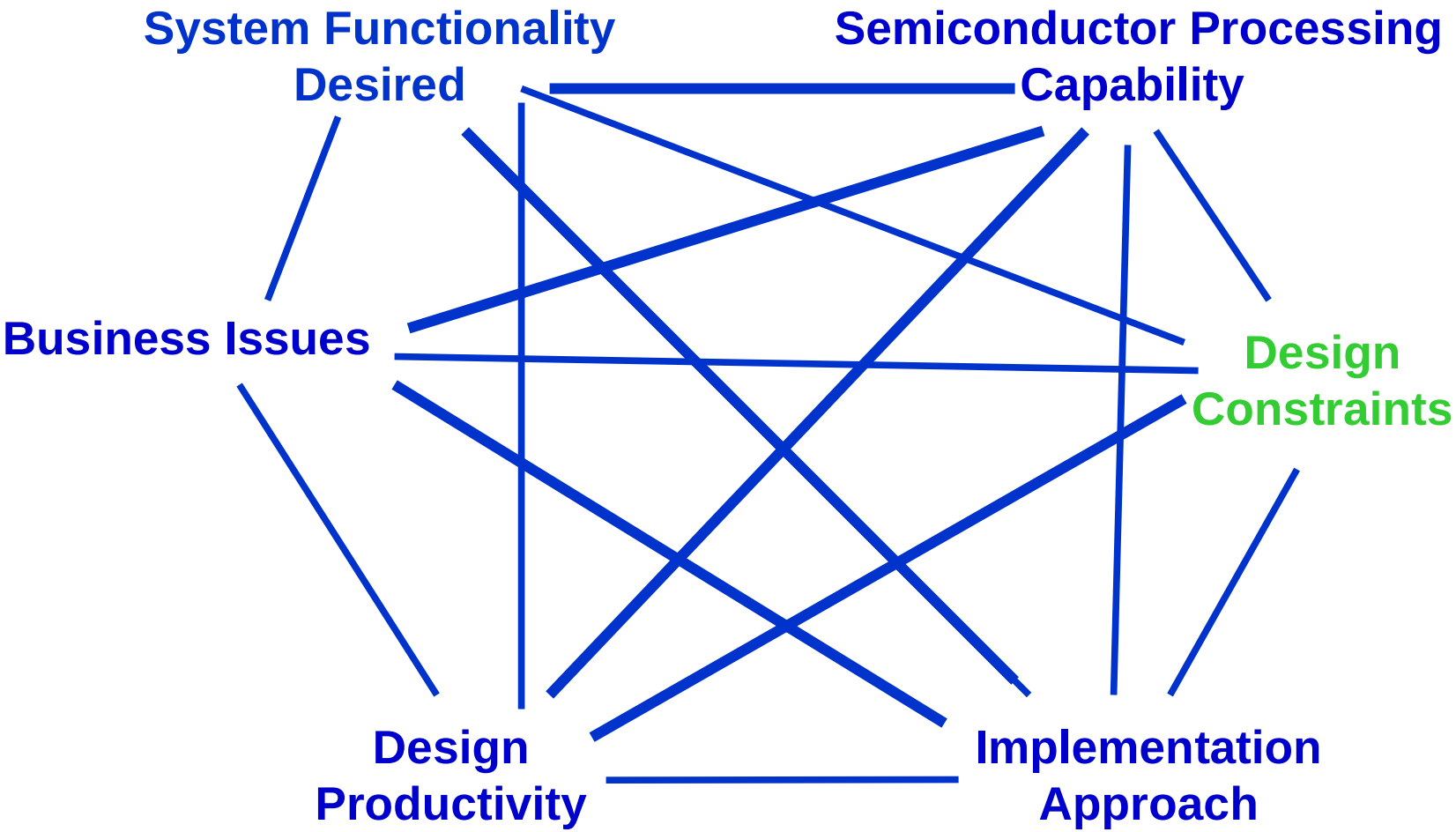
NTRS: Microprocessor: total transistors/chip



NRTS: Chip Frequency (Ghz)



Interrelationship of issues

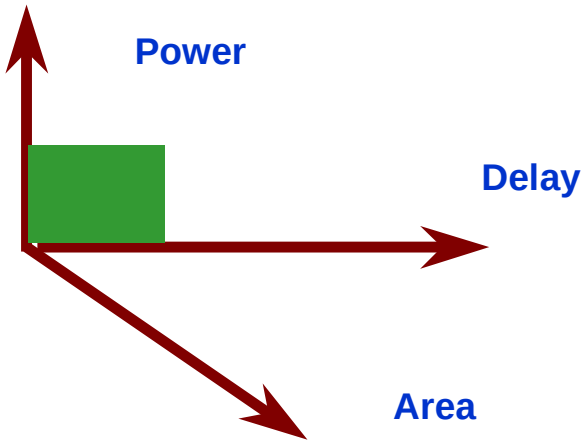


Design constraints

High-level (or low-level) system requirements get translated into specific design constraints for the integrated circuit

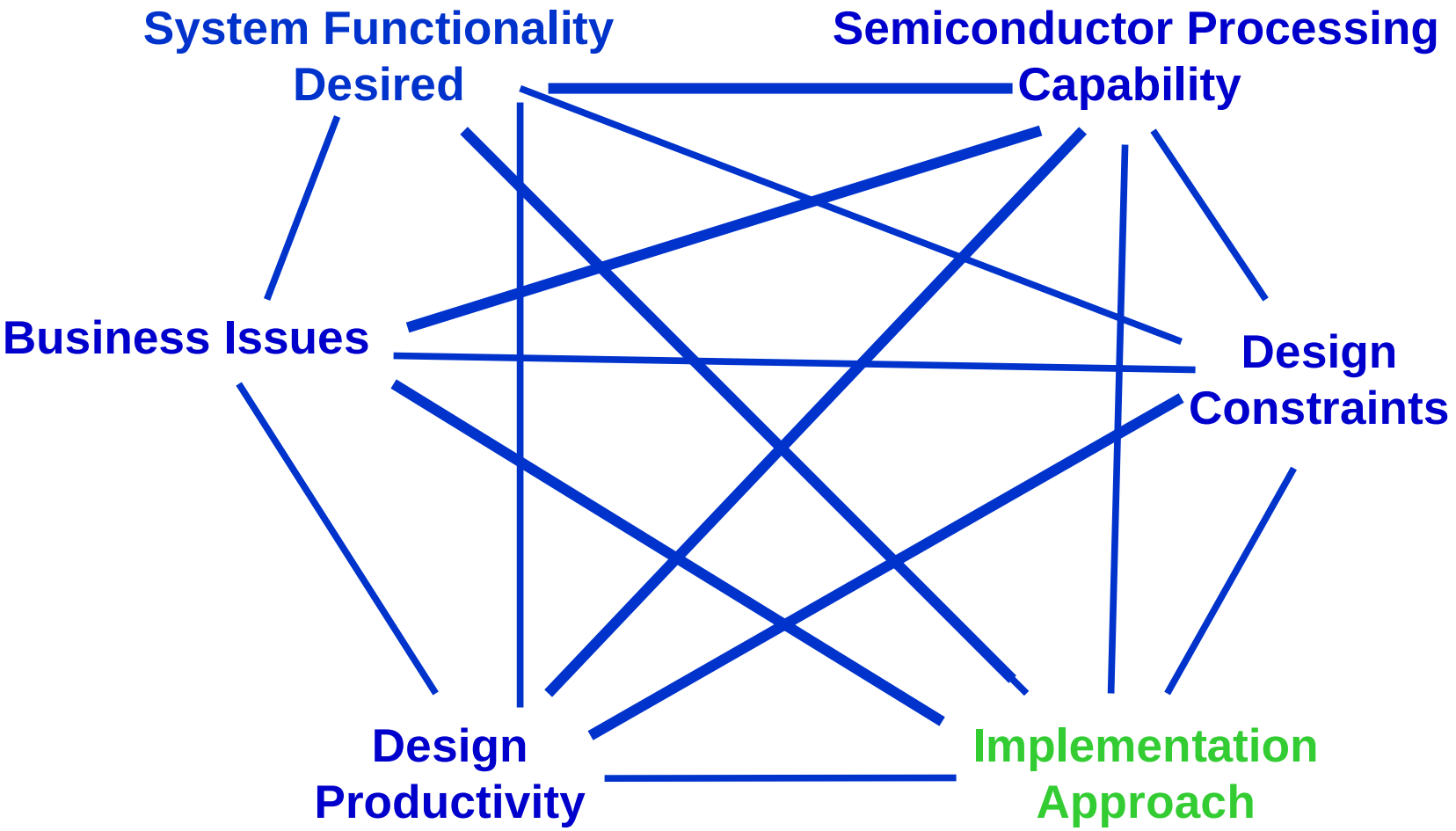
Primary factors are:

- Speed
  - To meet a standard - e.g. 66MHz.
  - To meet an internal system requirement - e.g. internal system bus speed of 200MHz.
  - To meet a specific market requirement - e.g. 800MHz.
- Power
  - To meet a system power dissipation limit - no fans!
  - To meet a chip cost limit - plastic package (1Watt)
  - To differentiate the product (higher MIPS/Watt)
- Chip area
  - directly related to chip cost
- Reliability
  - System constraints such as 1/10,000 defective boards get translated into IC constraints such as 1 defective part per million (1 DPM)



Failure to meet any one of these can lead to a failed IC project

Interrelationship of issues



Implementation Approaches

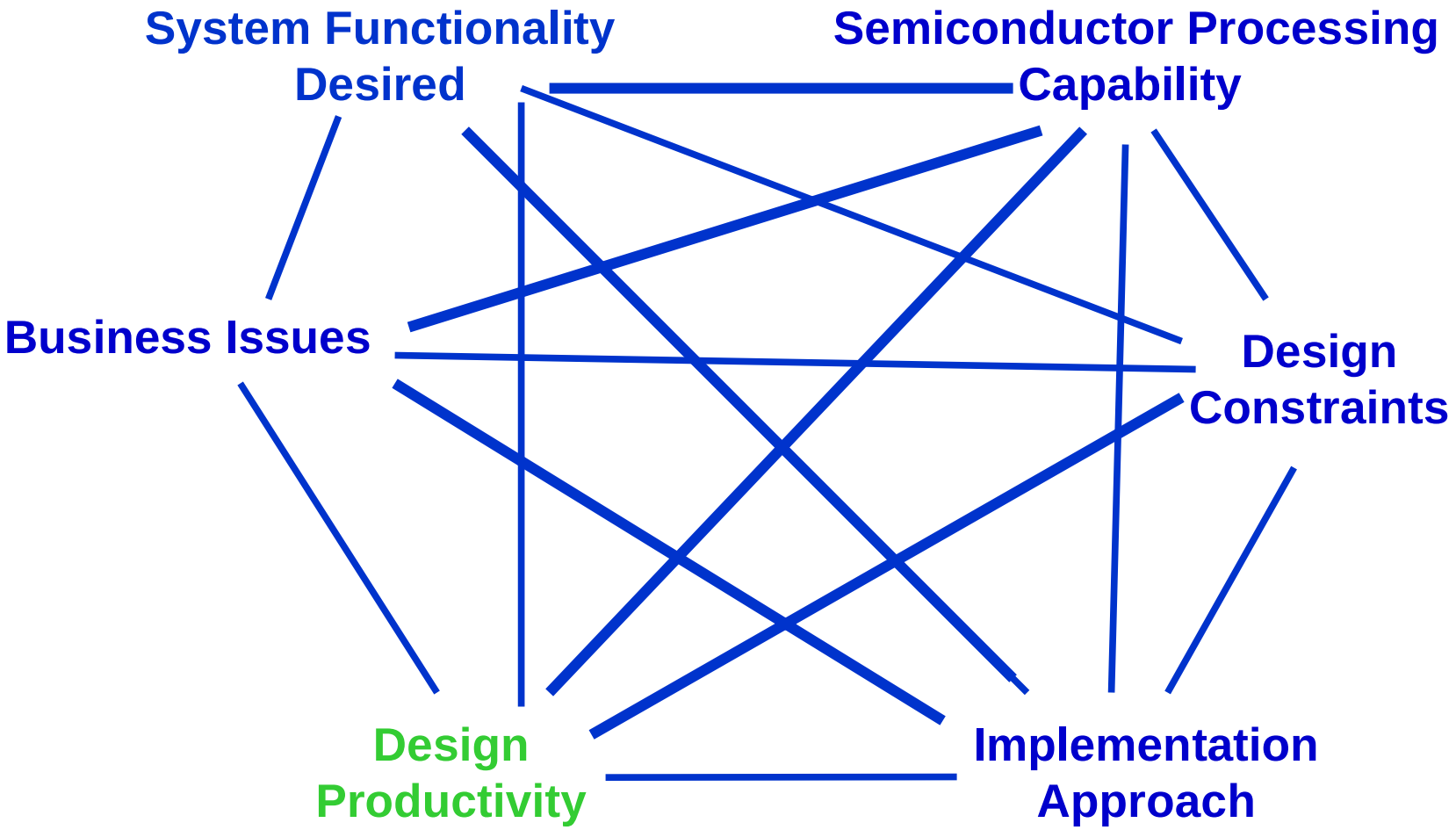
Software running on a

- **common microprocessor**
- **digital signal processor**
- **configurable-processor**
- **application-specific microprocessor**

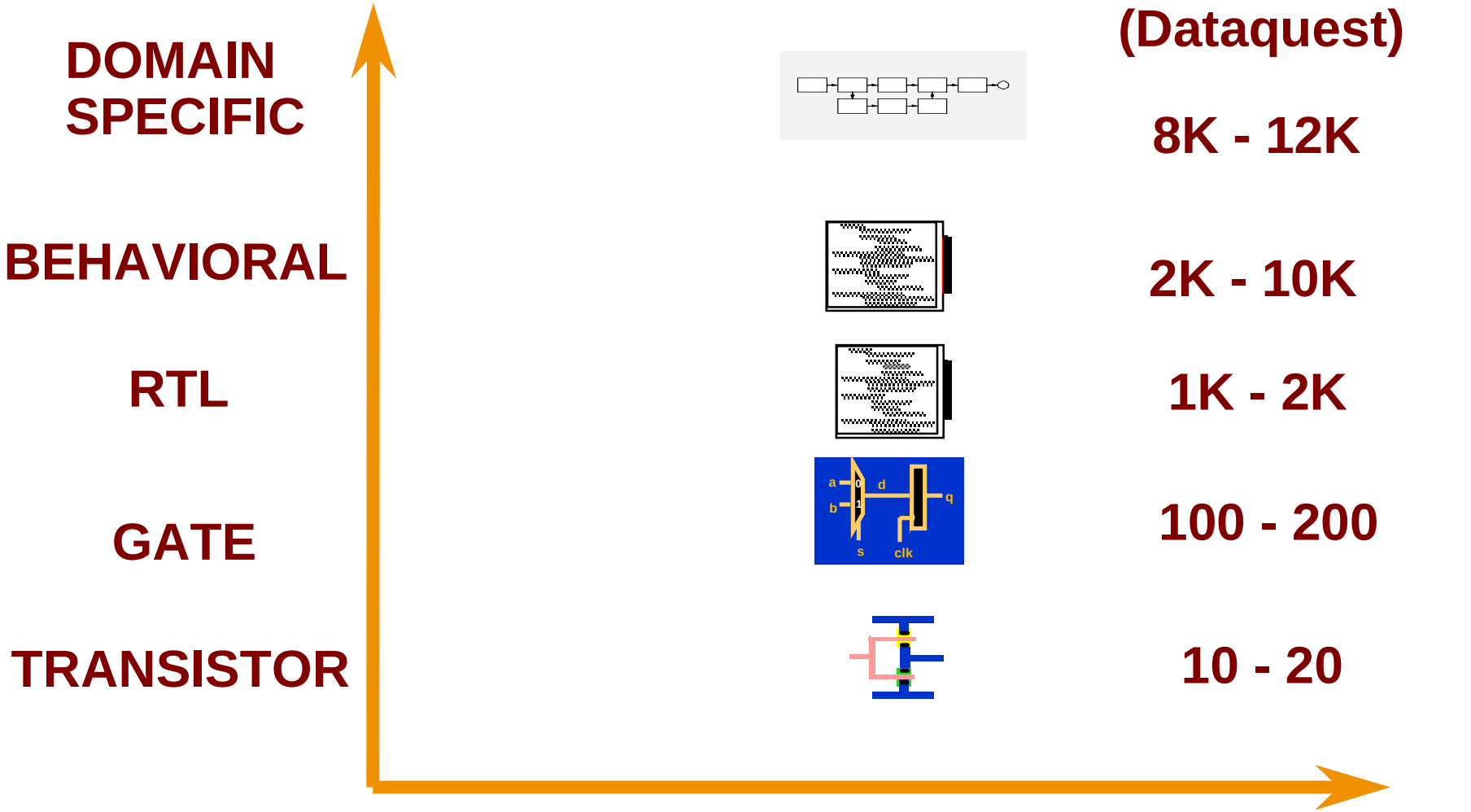
Hardware implementations

- **reconfigurable logic**
  - **static (FPGA)**
  - **dynamic**
- **standard-cell/gate-array**
- **``custom-logic''**

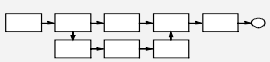
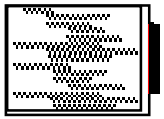
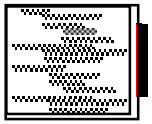
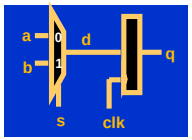
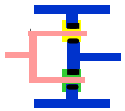
Interrelationship of issues



Design Productivity by Approach

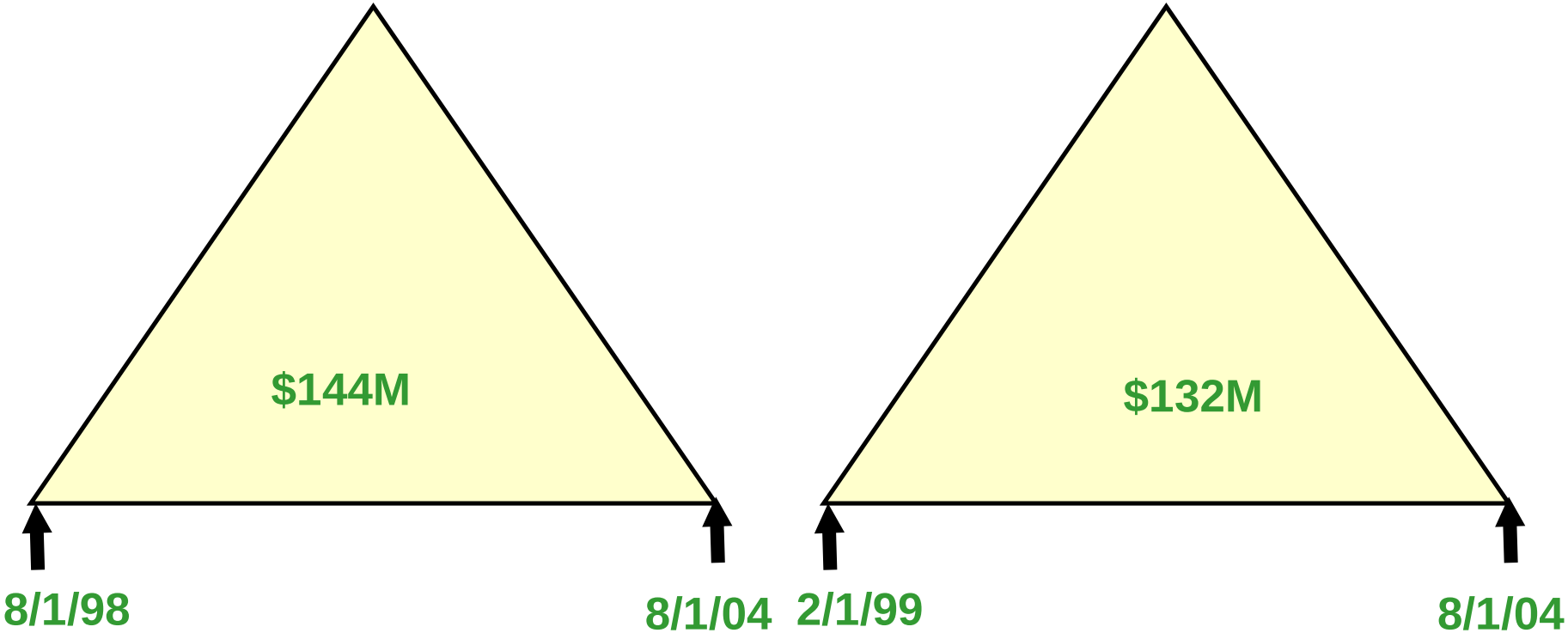


To Design, Implement, Verify ...

		10M tr/2.5M gates Staff Months	24M tr/6M Staff Months	64M tr/16M Staff Months
		62.5	150	400
Beh		125	300	800
RTL		625	1500	4000
gate		6250	15,000	40,000
tr		62,500	150,000	400,000

Why Productivity is Important 1:

What is the impact of 6 month delay in 6 year product cycle?



Find the fallacy in the picture above!

Why productivity is important 2:

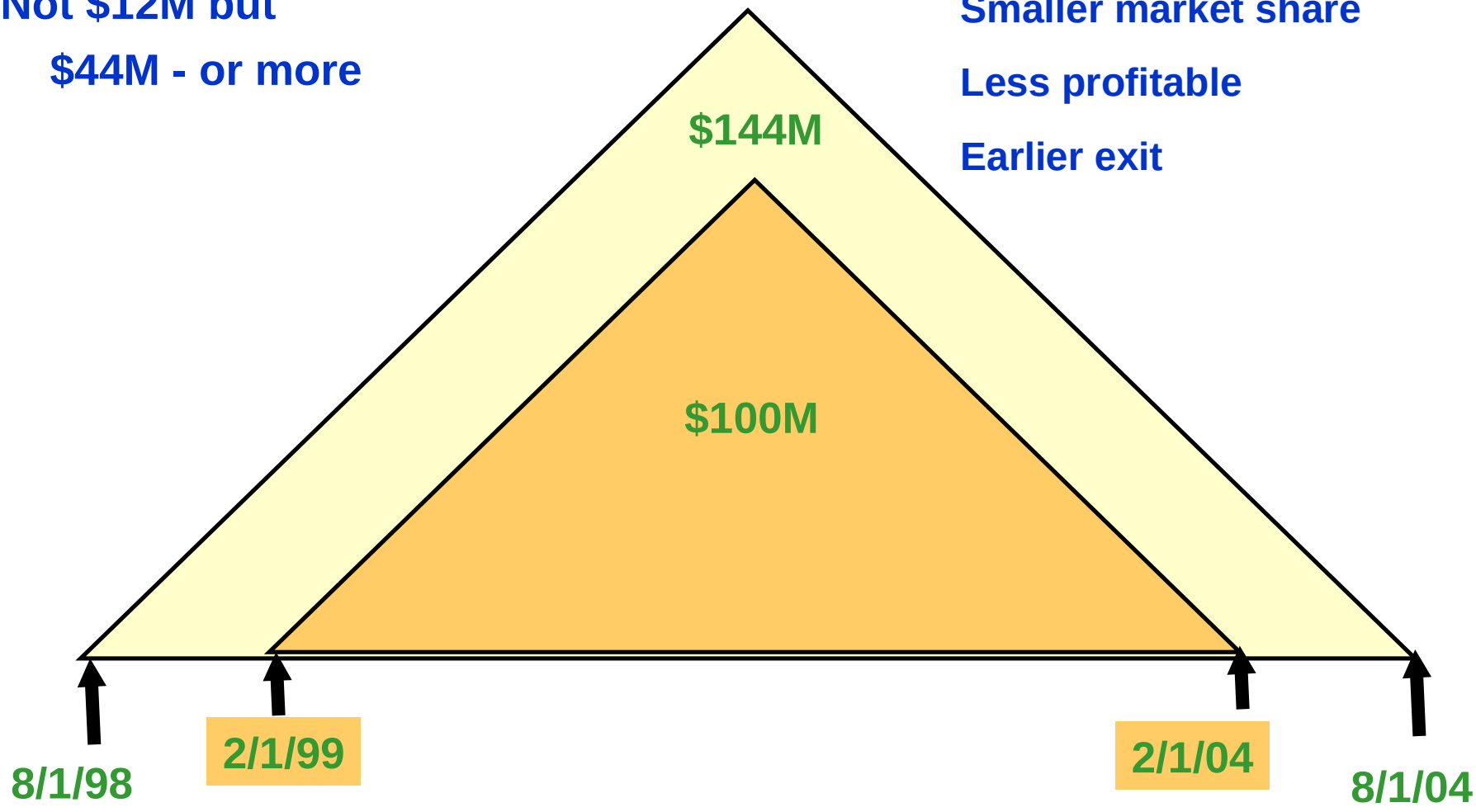
Not $12M but

$44M - or more

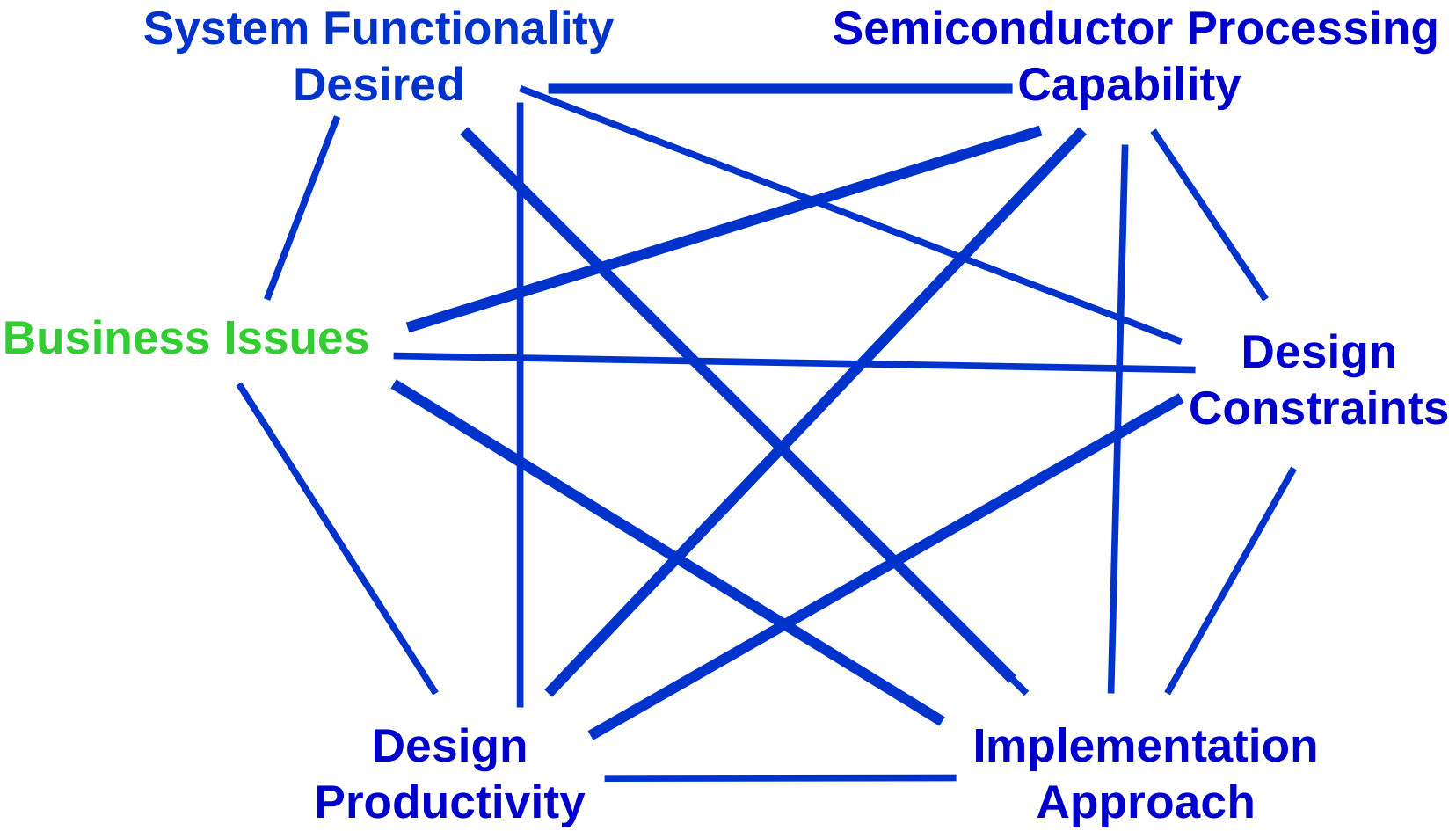
Smaller market share

Less profitable

Earlier exit



Interrelationship of issues



Business Issues

- A significant piece of intellectual property (e.g. microprocessor core) may be ``thrown in'' if you use a particular semiconductor facility (e.g. Motorola) in high volume (e.g. laser printer engine
- IP components may be available to a company due to large ``patent portfolio swaps'' between major manufacturers (e.g. Lucent, IBM, TI)
- There is an emerging legal world of 3rd Party IP licensing