EE290 A: Advanced Topics in CAD
Component Based Design of Electronic Systems
Lecture 4

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HW1: Back of Envelope Implementation of JPEG

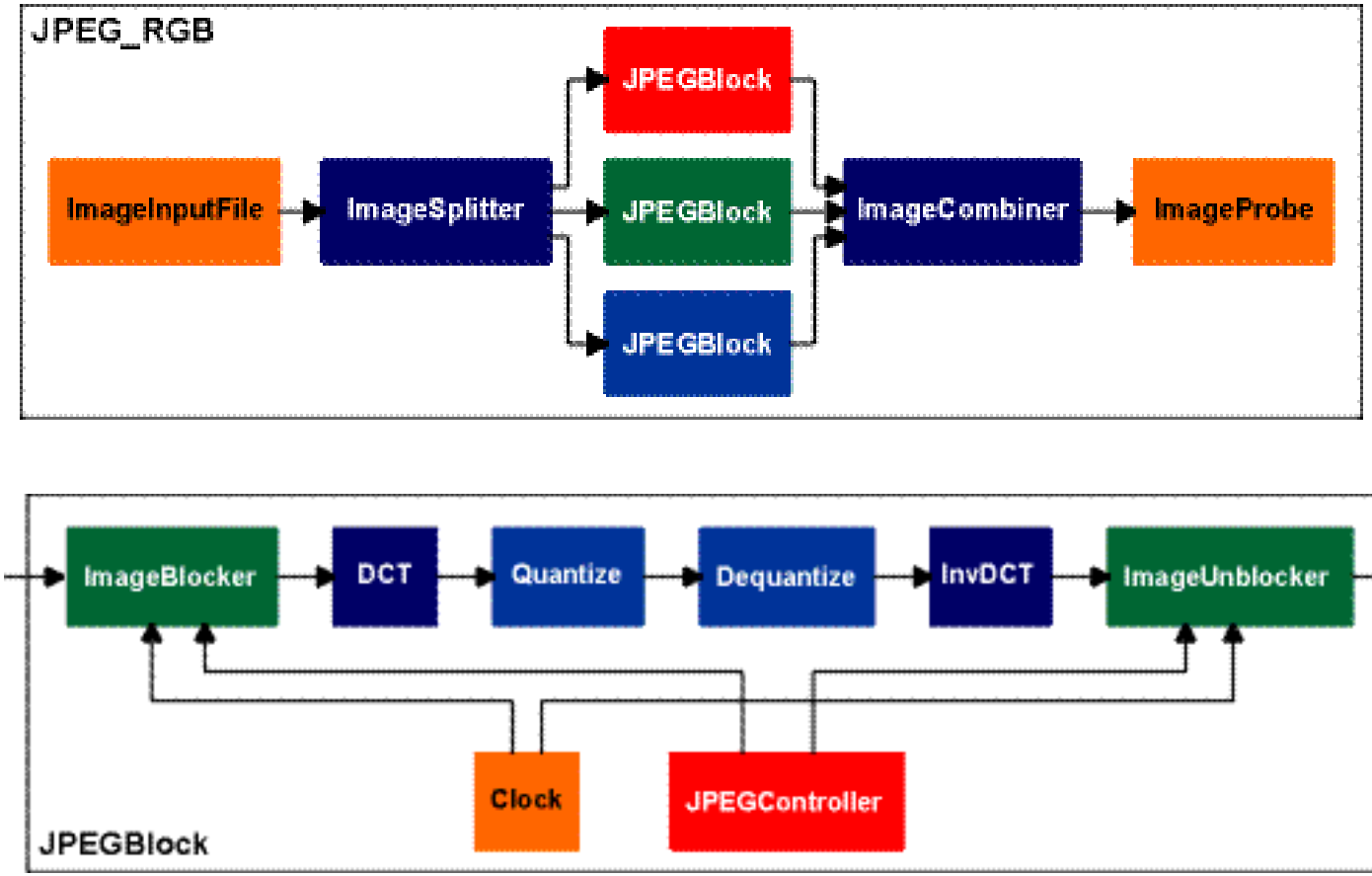
Software running on a

- **common microprocessor**
- **digital signal processor**
- **configurable-processor**
- **application-specific microprocessor**

Hardware implementations

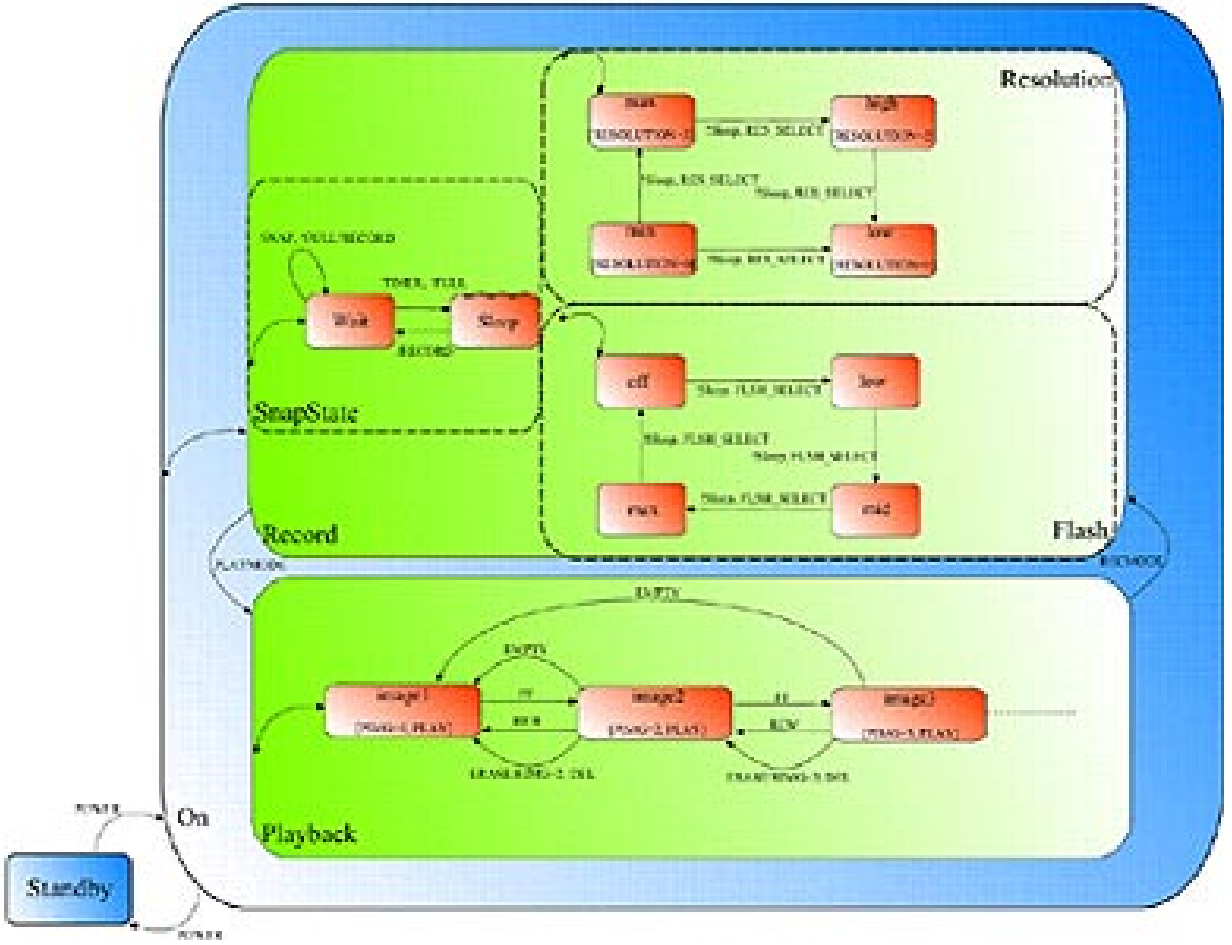
- **reconfigurable logic**
  - **static (FPGA)**
  - **dynamic**
- **standard-cell/gate-array**
- **``custom-logic''**

JavaTime JPEG Organization



Example: Digital Camera Controller

Digital camera controller described as hierarchical finite state machine.



Homework 1: Determine for JPEG

Performance:

- **clock speed (e.g. 200 MHz.)**
- **execution performance in intended operation (e.g. 100 frames/sec)**

Power dissipation

- **in operation (dynamic/static) (e.g. .7Mw)**
- **per mm^2 (power density) (e.g. .34 Mw)**

Cost:

- **Die size (name process generation): (e.g. .3mm x .4mm in 250nm)**
- **if you don’t have data on 250nm - extrapolate using scaling**

What do we get from HW 1?

Initial familiarity with what an IP block is

Familiarity with implementation alternatives

Key parameters for the quality of an IP block

How to estimate the quality

…

Later we will learn how important (and hard) it is to estimate accurately!!

Homework 2: Identify individual components

Processor cores:

- **microprocessor**
- **DSP**
- **microcontroller**

Standard interfaces:

- **PCI**
- **Ethernet**

Application specific components

- **MPEG decoder**
- **JPEG encoder/decoder**

Smaller building blocks?:

- **Viterbi, IDCT/DCT, Motion estimation**

Where to find them?

http://www.mentor.com/inventra/cores/index.html

Homework 2: Determine for the IP

How is the IP described? How is it delivered?

Performance:

- **clock speed (e.g. 200 MHz.)**
- **execution performance in intended operation (e.g. 100 frames/sec)**

Power dissipation

- **in operation (dynamic/static) (e.g. .7Mw)**
- **per mm^2 (power density) (e.g. .34 Mw)**

Cost:

- **Die size (name process generation): (e.g. .3mm x .4mm in 250nm**
- **cost to license, buy etc. (e.g. 20K, or $2M licence, $1 per die royalty)**

Homework 2: Determine for the IP

How is it delivered? How is it intended to be used:

- **SW**
  - **pure SW, SW IP**
  - **SW running on a targeted processor**
- **HW**
  - **hard - actual layout**
  - **firm - netlist**
  - **soft - synthesizable RTL model in VHDL?/ Verilog?**
- **reconfigurable**

Who sells it?

- **Vertical semiconductor company - TI, Motorola, IBM**
- **3rd Party IP supplier - ARM, Mentor: Inventra**

Estimate of Non-recurring engineering costs of developing IP

Sources of your information

What do we get from HW 2?

Broader familiarity with what an IP block is

Sense of growing IP industry

Sense of distribution of implementation alternatives

Key parameters for the quality of an IP block

…

We will use the results of HW 2 to identify the block of IP that we use for HW 3. JPEG is the default.

HW3: Real Implementation of class IP block

Software running on a

- **common microprocessor**
- **digital signal processor**
- **configurable-processor**
- **application-specific microprocessor**

Hardware implementations

- **reconfigurable logic**
  - **static (FPGA)**
  - **dynamic**
- **standard-cell/gate-array**
- **``custom-logic''**

Homework 3: Determine for your impl.

Performance:

- **clock speed (e.g. 200 MHz.)**
- **execution performance in intended operation (e.g. 100 frames/sec)**

Power dissipation

- **in operation (dynamic/static) (e.g. .7Mw)**
- **per mm^2 (power density) (e.g. .34 Mw)**

Cost:

- **Die size (name process generation): (e.g. .3mm x .4mm in 250nm)**
- **if you don’t have data on 250nm - extrapolate using scaling**

Homework 3: In your implemenation

Document the design flow that you use:

- **SW**
  - **standard C development flow**
  - **assembly-language coding**
  - **configurable processor tools**
- **HW**
  - **RTL synthesis design flow into standard cell**
  - **custom design flow into layout**
  - **FPGA design flow**
- **Describe the tools that you use to estimate/measure the quality of your implementation**
  - **speed, power, area**
- **Estimate design time to do the implementation**
- **How representative is your implementation?**
  - **How could you improve your implementation**
  - **How far off from ``optimal'' is it?**

Class Project - Homework 4

What we get from homework 3 is homework 4 ;-)

Compare the type of implementations on the key dimensions:

Quality of results

- **Performance:**
  - **clock speed (e.g. 200 MHz.)**
  - **execution performance in intended operation (e.g. 100 frames/sec)**
- **Power dissipation**
  - **in operation (dynamic/static) (e.g. .7Mw)**
  - **per mm^2 (power density) (e.g. .34 Mw)**
- **Cost:**
  - **Die size (name process generation): (e.g. .3mm x .4mm in 250nm**

Productivity/Time-to-market

- **Design effort in implementation**

Predictability

Portability

Are the quality of results advantages of a particular approach consistent with the design time costs?

Outline of issues

Why components?

- **Raw silicon capability**
- **Design productivity**

What type of components?

- **What size of component?**
- **What type/capability of component?**

How will they be designed?

- **Review of implementation alternatives**
- **Review of common design flows**

Who are the players?

- **foundries,**
- **fabless semiconductor, 3rd party IP providers, vertical semiconductor,**
- **system companies**

Which design styles are likely to predominate

- **Time-to market (productivity)**
- **Features**
  - **Process portability**
  - **In-field up-gradabilty, programmability**
  - **Quality of results**

Interrelationship of issues