Integration Architecture Overview

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(Systems-ON-ICS)

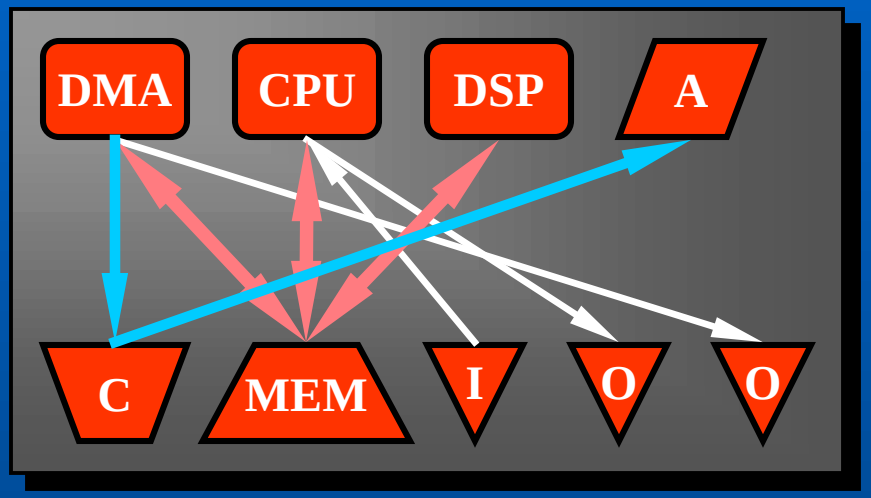
Overview

- ***Introduction***
- **Architecture Overview**
- **Implementation**
- **Example**
- **Summary**

SOC Applications and Data Flow

APPLICATION AREA
DIGITAL CAMERA
COLOR PRINTERS
NEXT GENERATION STB
NETWORK SWITCHING
SOHO MULTIMEDIA XDSL INTERFACE
DIGITAL TELEVISION
DIGITAL VIDEO SERVER
WORLD PHONE

SOC Data Flow

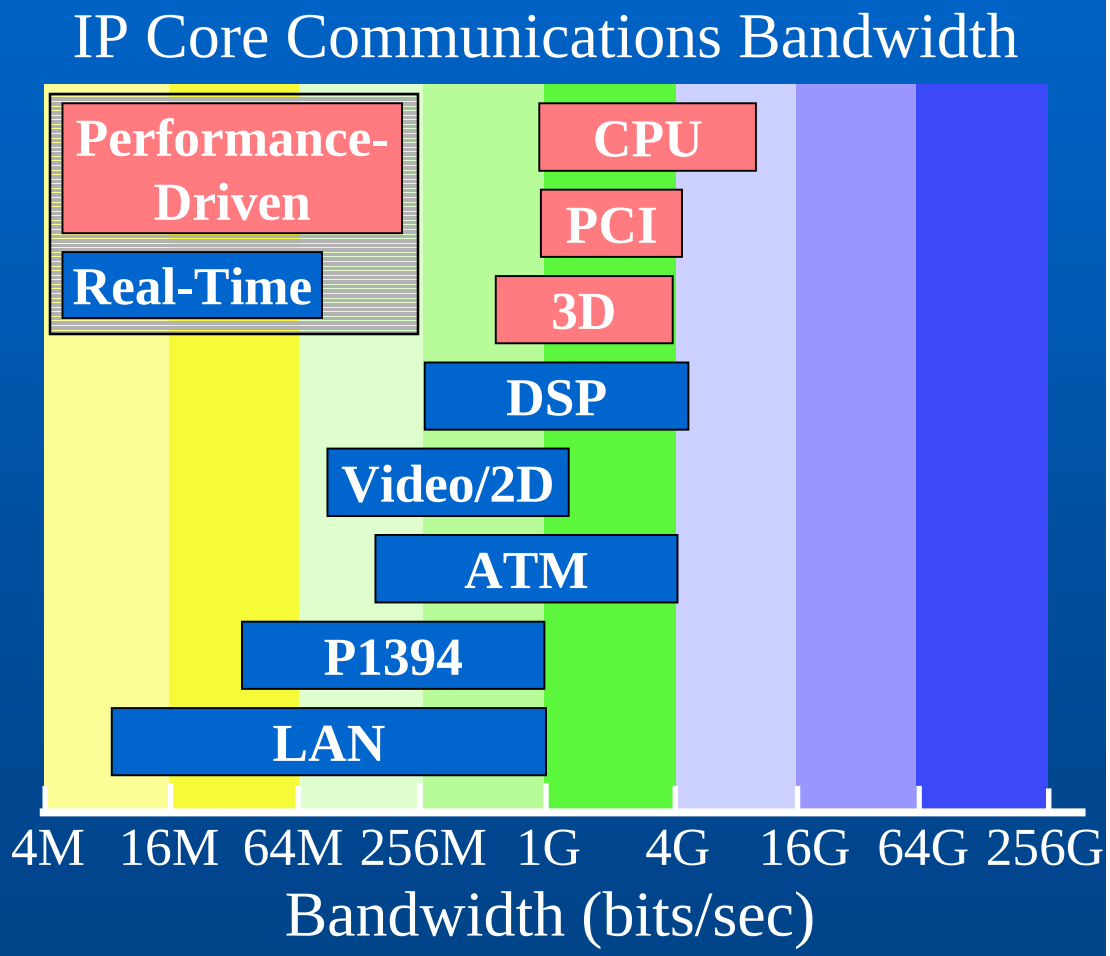


System-on-a-Chip Communications

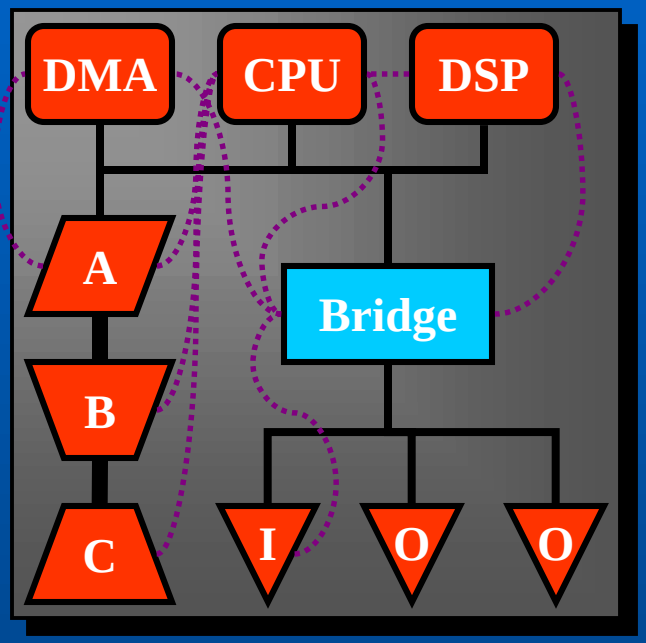
Characteristics:

- **Wide performance range**
- **Increasing real-time multimedia/networking traffic**
- **Shared memory requirements**
- **Complex interactions**

Challenging Design



Conventional Approach



SOC Design Requirements

- New design for each ***system***
- Match ***system*** design cycle

- Hit cost/performance goals

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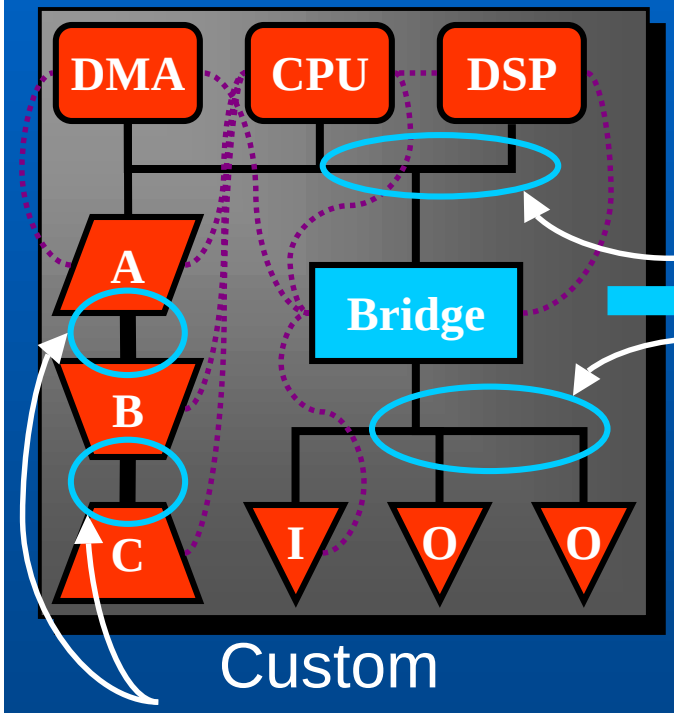
Sonics Integration Architecture

Conventional

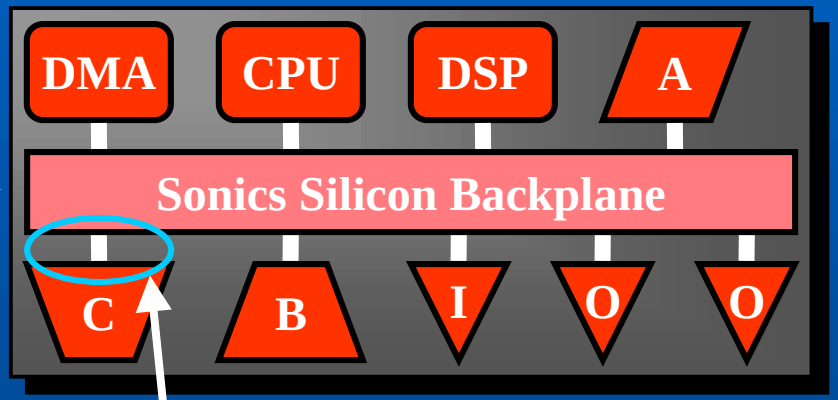


System Bus

Peripheral Bus

Custom Interfaces

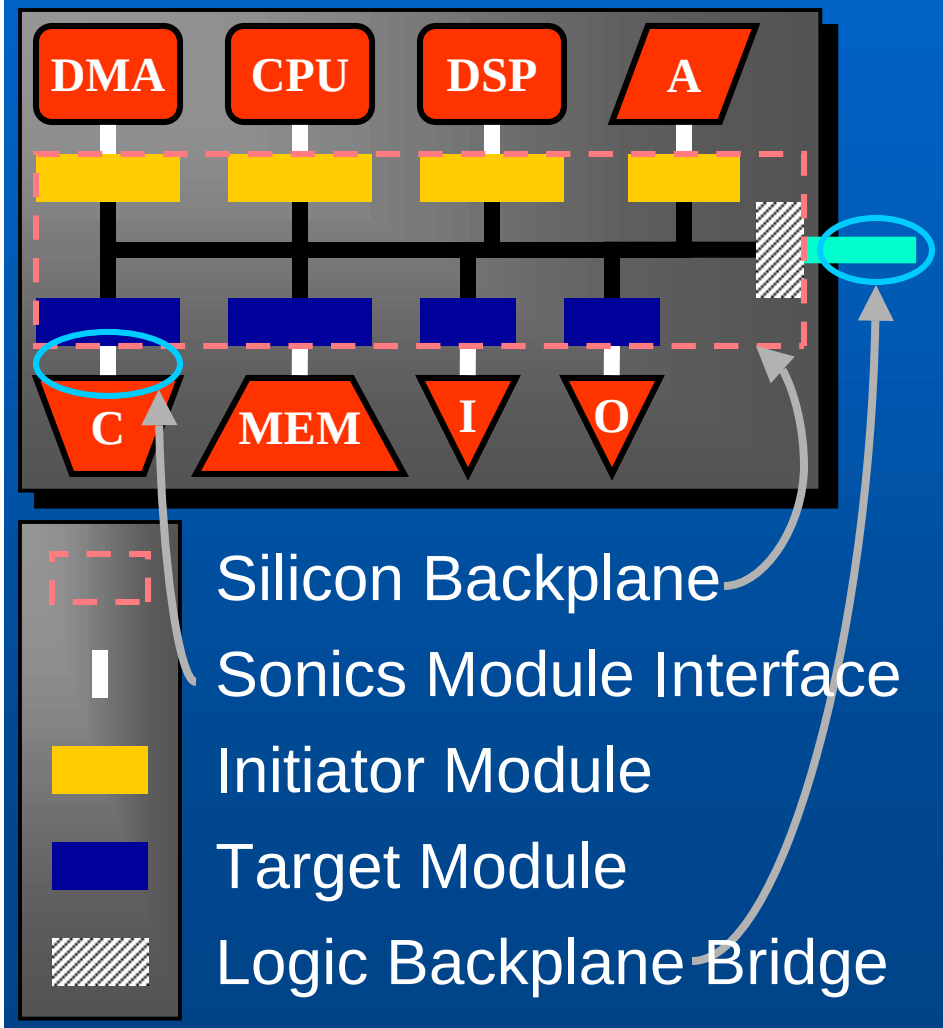
Sonics Integration Architecture



Sonics Module Interface

Allows unification of *all* on-chip communication

Integration Architecture Aspects*



- Tunable Communications Subsystems
  - Silicon Backplane™
  - Logic Backplane™
- Configurable IP Core Interface
  - Sonics Module Interface
- Design Software
  - Backplane Compiler

* Patent Pending

SONICS, INC.

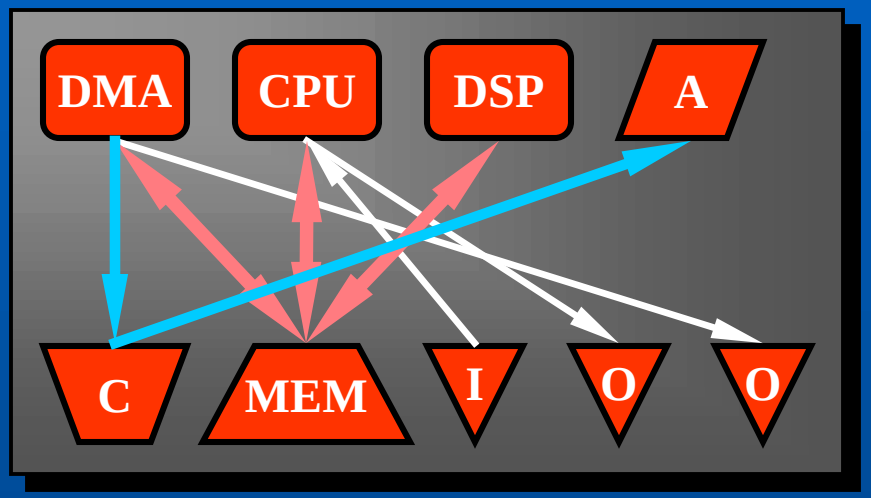
Bus Bandwidth Requirements

- **Must satisfy sum of *sustained* BW**
- **Total bus BW > *peak* BW of any IP Core**

Bandwidth *mismatch* between Bus and IP Cores

Need *de-coupled* Bus performance

SOC Data Flow

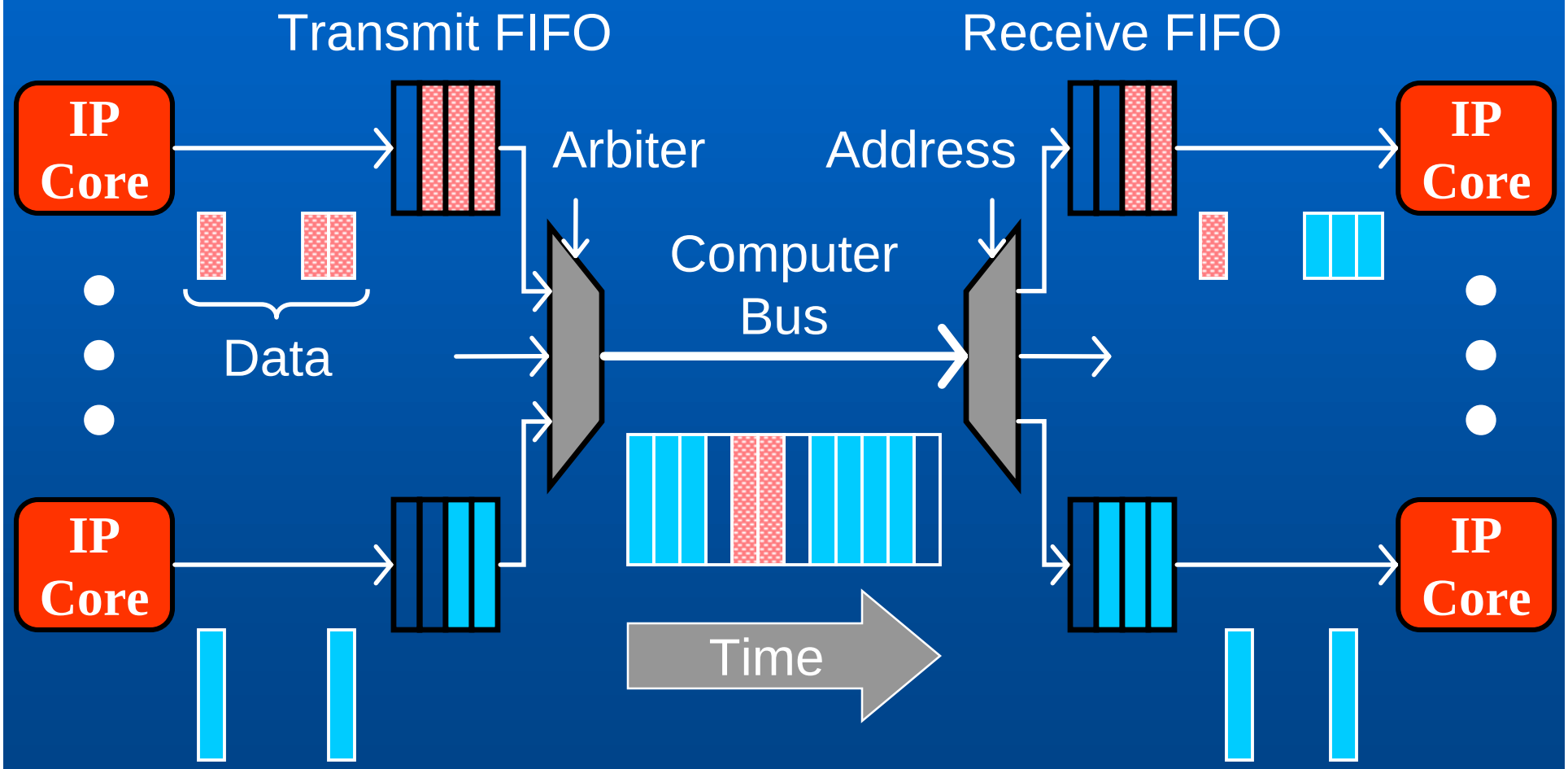


< 10 Mbits/sec

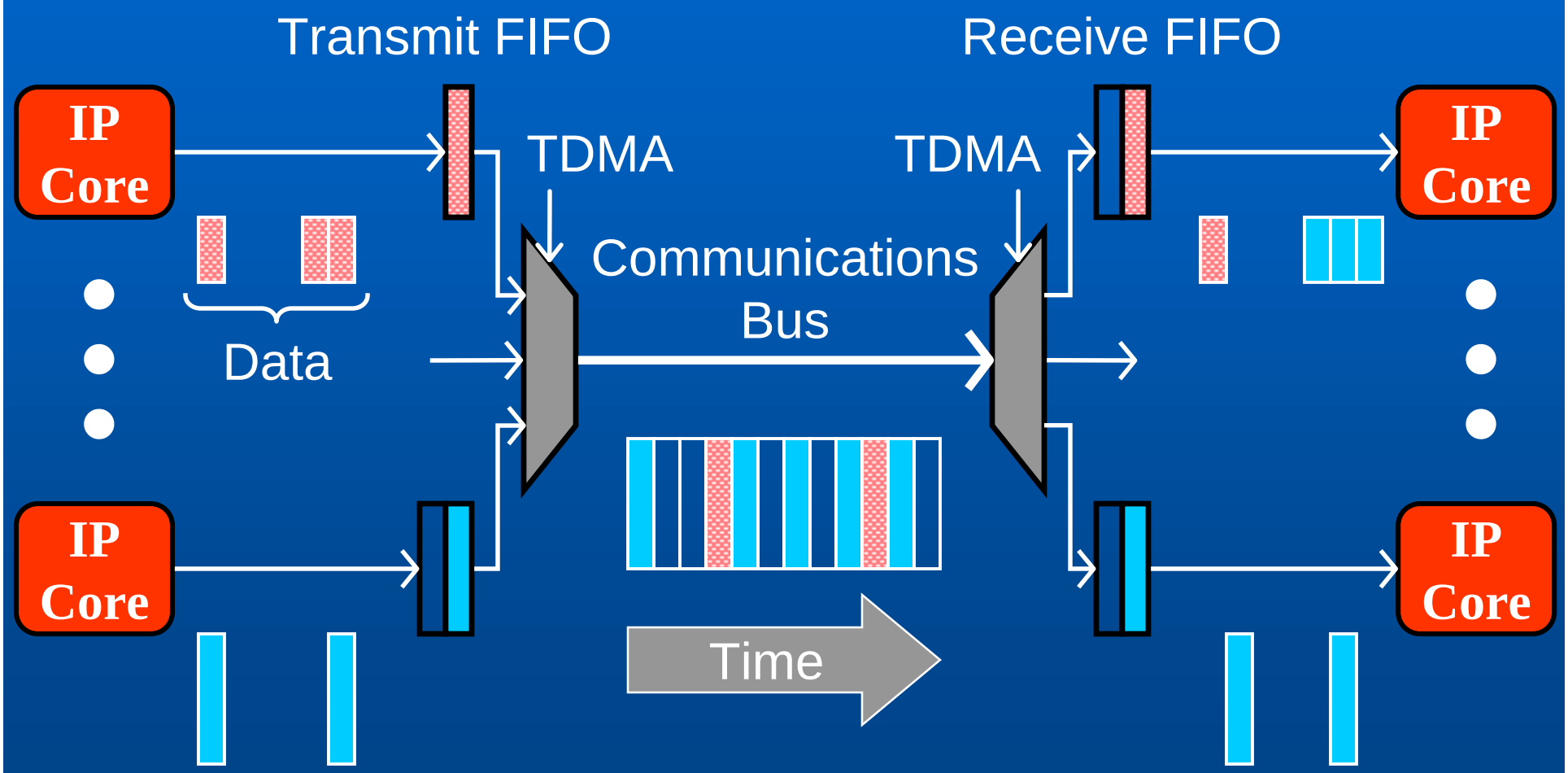
< 100 Mbits/sec

> 100 Mbits/sec

Computer Bus Approach



Communication Bus Approach



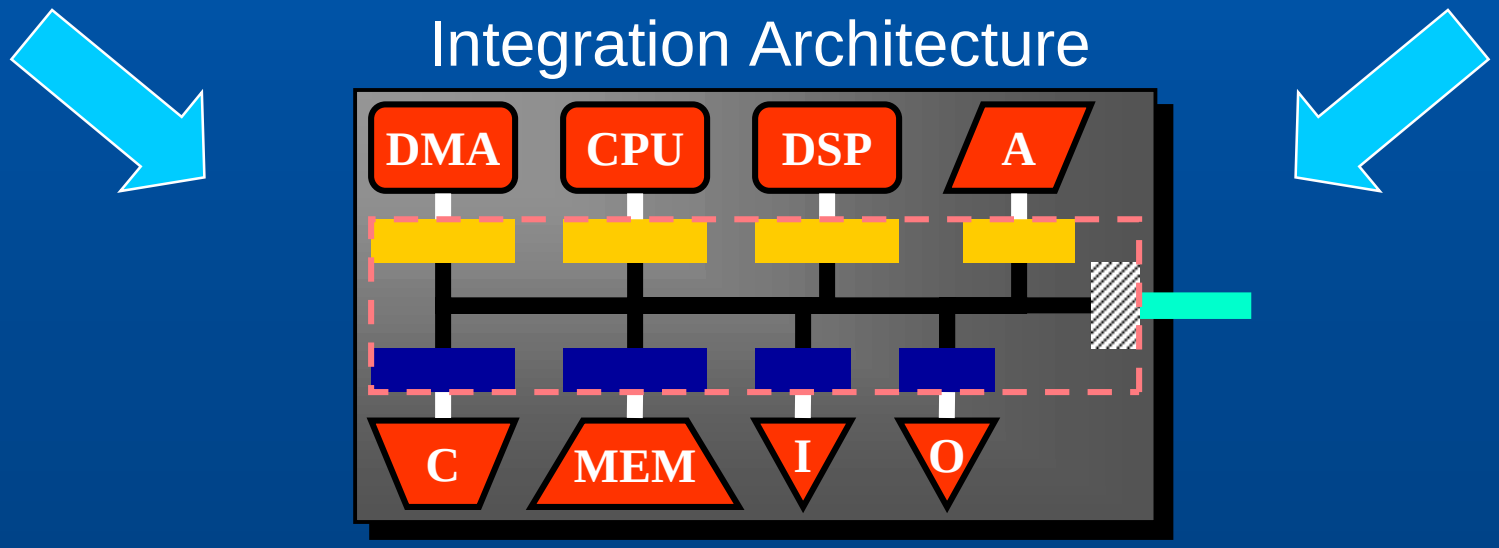
Integration Architecture Features

From Computing

- Address-based Selection
- Write *and* Read Transfers
- Pipelining

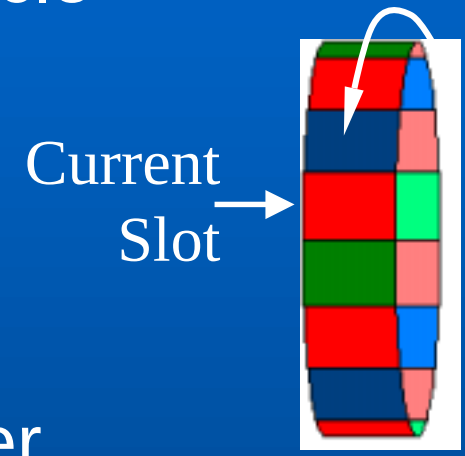
From Communications

- Efficient BW De-coupling
- Guaranteed BW & Latency
- Side-band Signaling

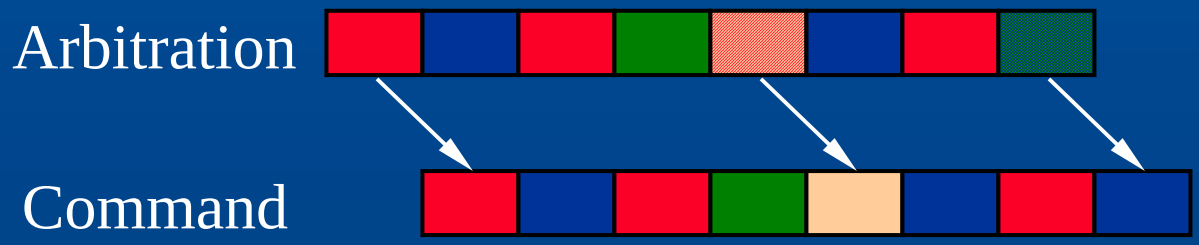


Guaranteed Bandwidth Arbitration

- Independent arbitration for **every** cycle
- Two phases
  - Distributed TDMA
  - Round robin



Gives SOC designer fine control over system bandwidth



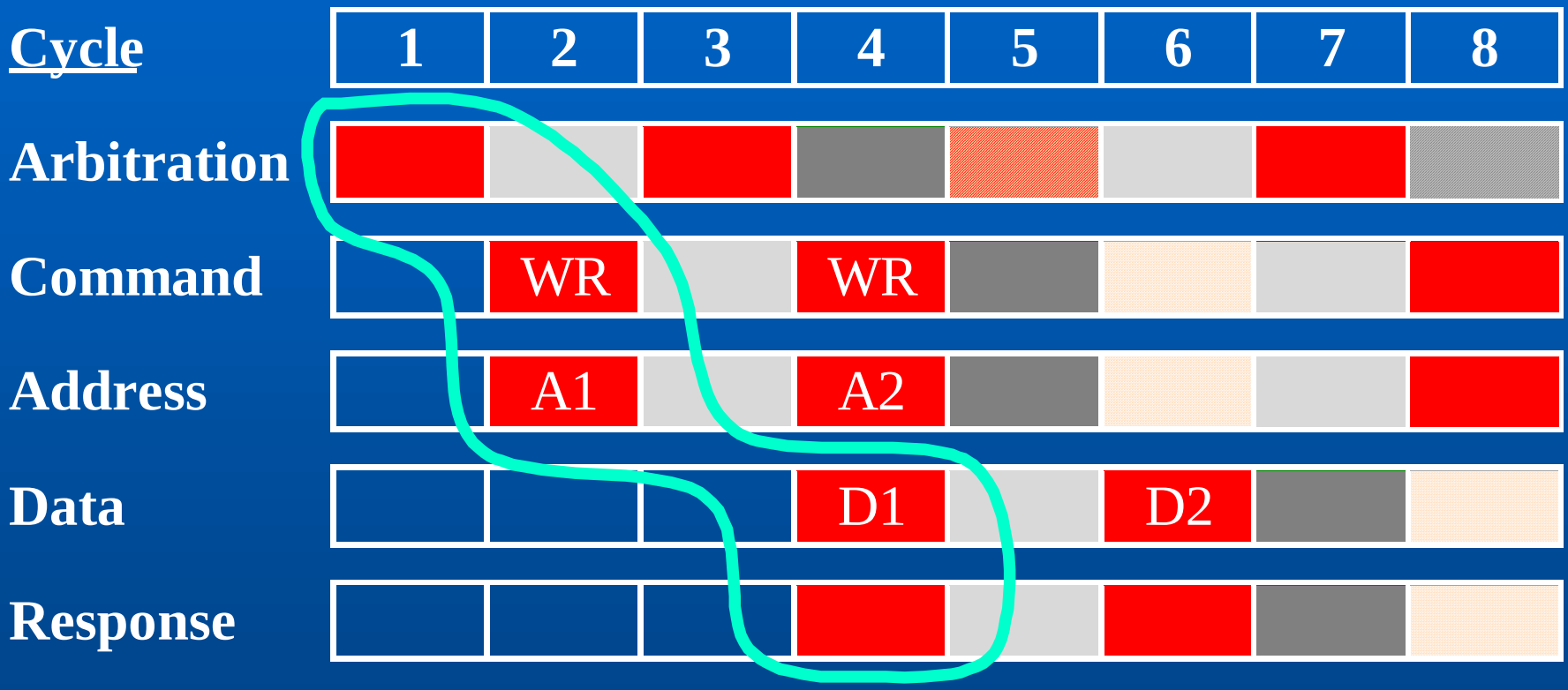
Guaranteed Latency

- Fixed latency between command/address and data/response phases
- Matches pipelined CPU model
  - High performance access to on-chip resources
- Allows routing of pipelined data through Backplane
- Latency is re-programmable in software
- Variable-latency IP Cores do ***not*** tie up the Backplane

Memory-Mapped Address Space

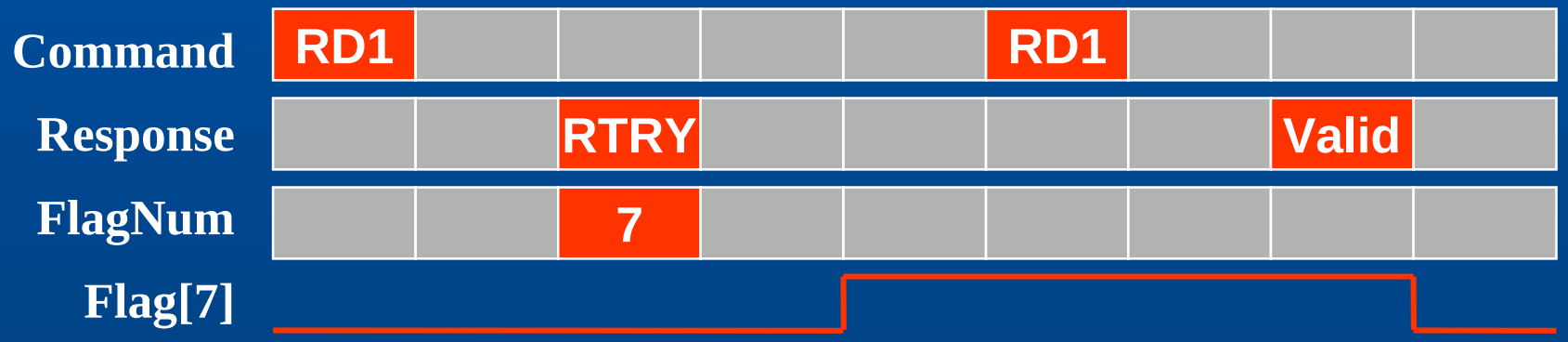
- IP Cores accessed ***only*** via Read / Write commands
- Interface Modules decode addresses for IP Core selection
- Interface Module address match logic features:
  - Variable match width
  - Multiple match regions
  - Positive / Negative decoding
  - Subtractive decoding
- Module Configuration Registers
  - Access re-programmable / hardwired Backplane features
  - IP Core device control registers

Pipeline Diagram

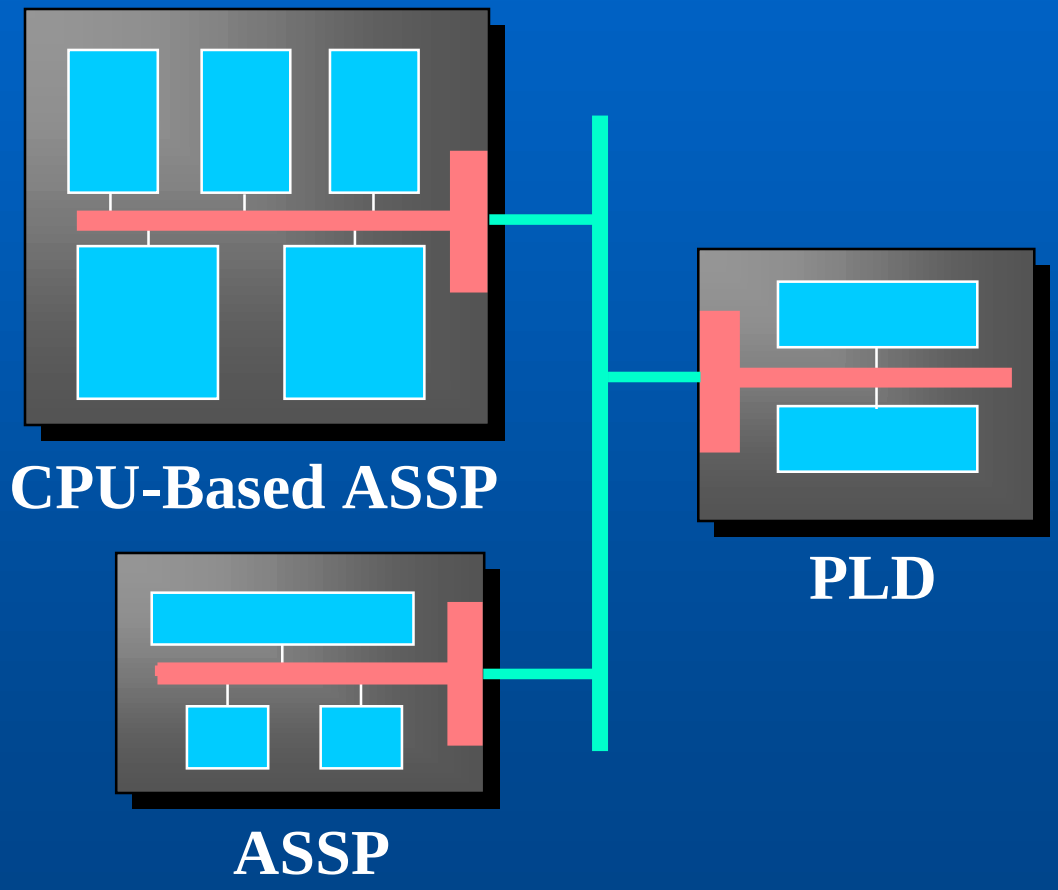


Integrated Signaling Mechanism

- Dedicated Backplane wires (**`Flags`**) support:
  - Bus-style Out-of-Band Signaling (Interrupts)
  - Point-to-Point Communications (Flow control)
  - Dynamic point-to-point (Retry mechanism)
- Integral part of Integration Architecture
  - Same design flow, timing, flexibility as address/data part
- Retry Mechanism:



Off-Chip Extension: Logic Backplane



Silicon Backplane

Logic Backplane

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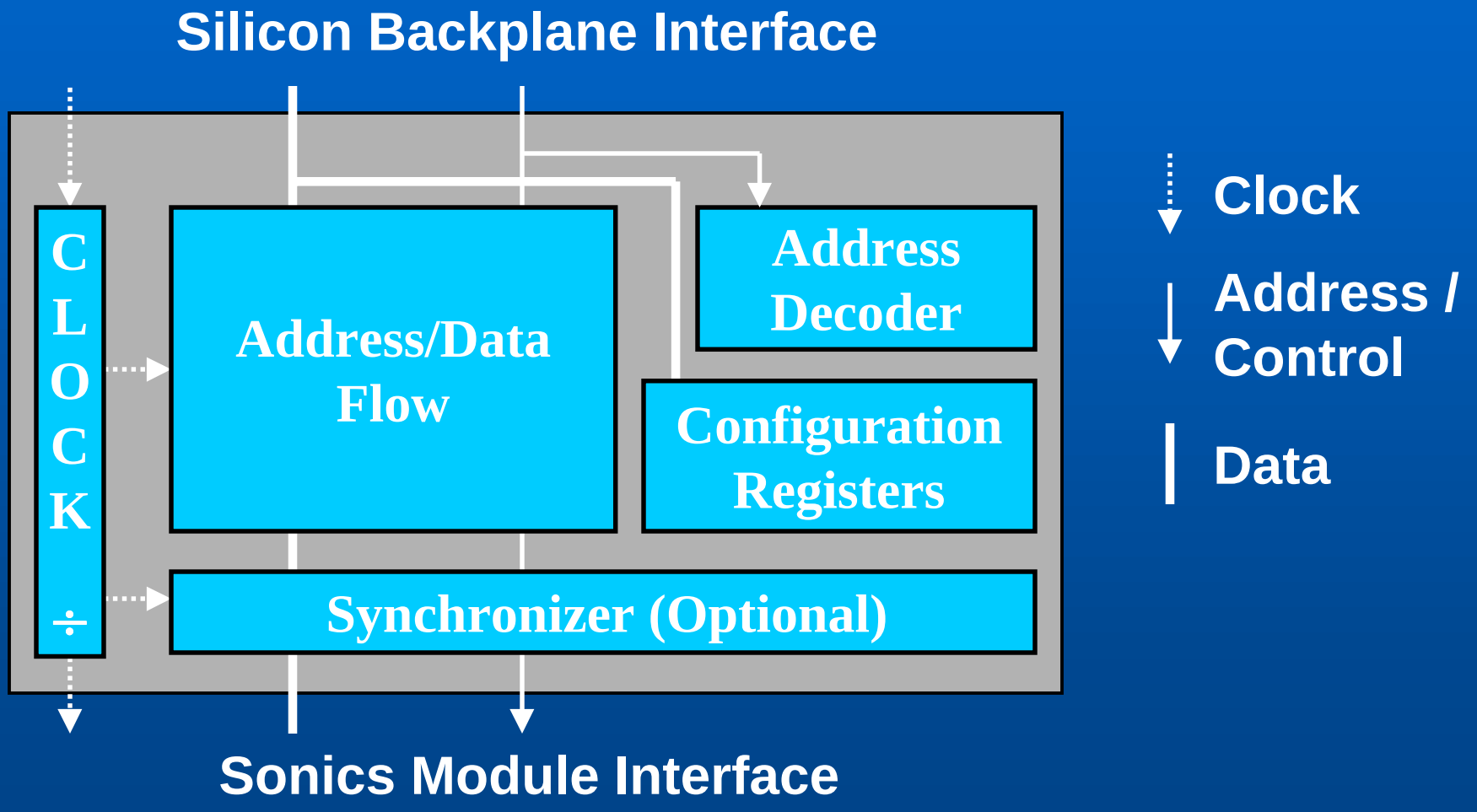
Target Module Block Diagram

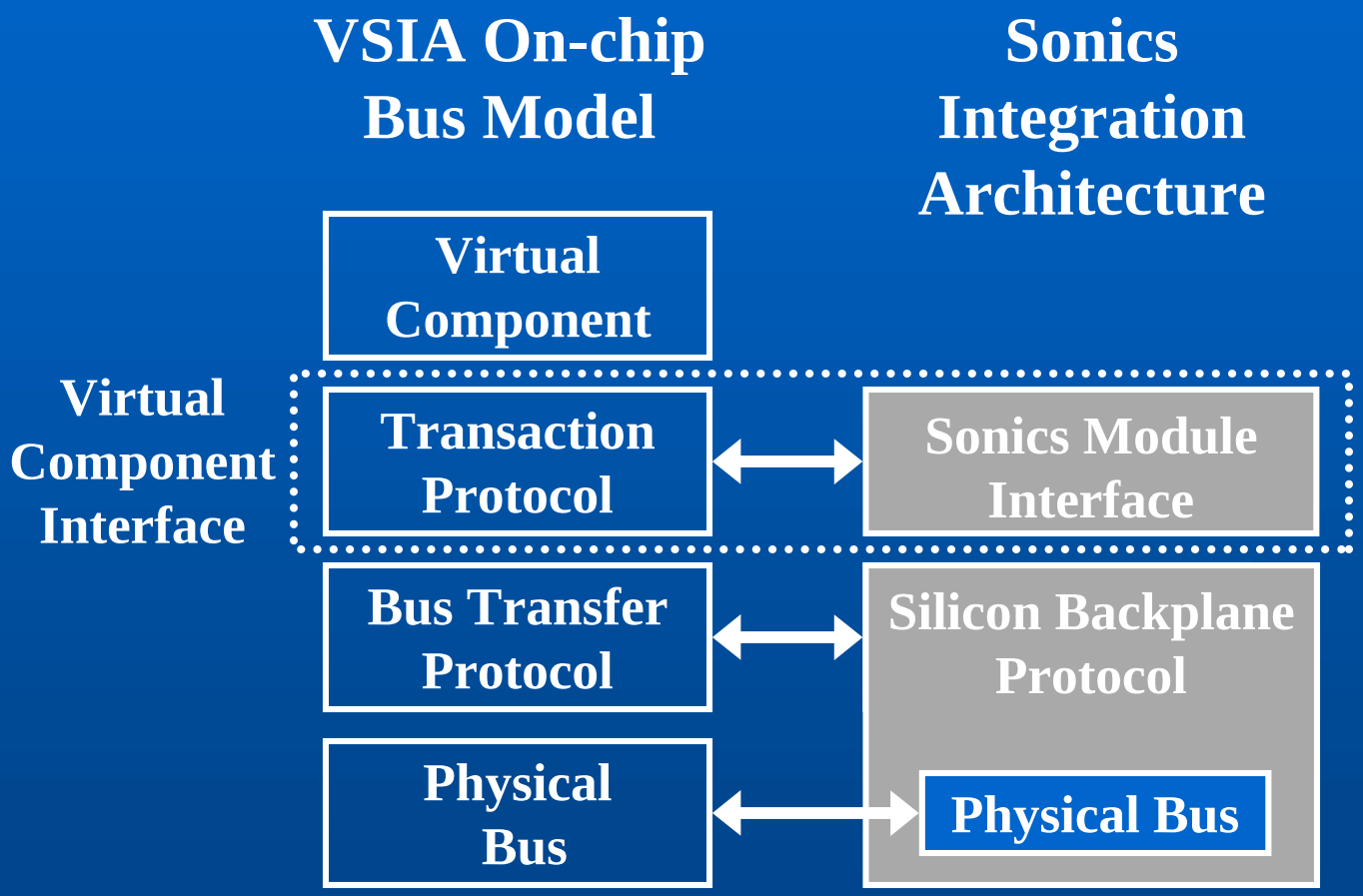


Sonics Module Interface: Basics

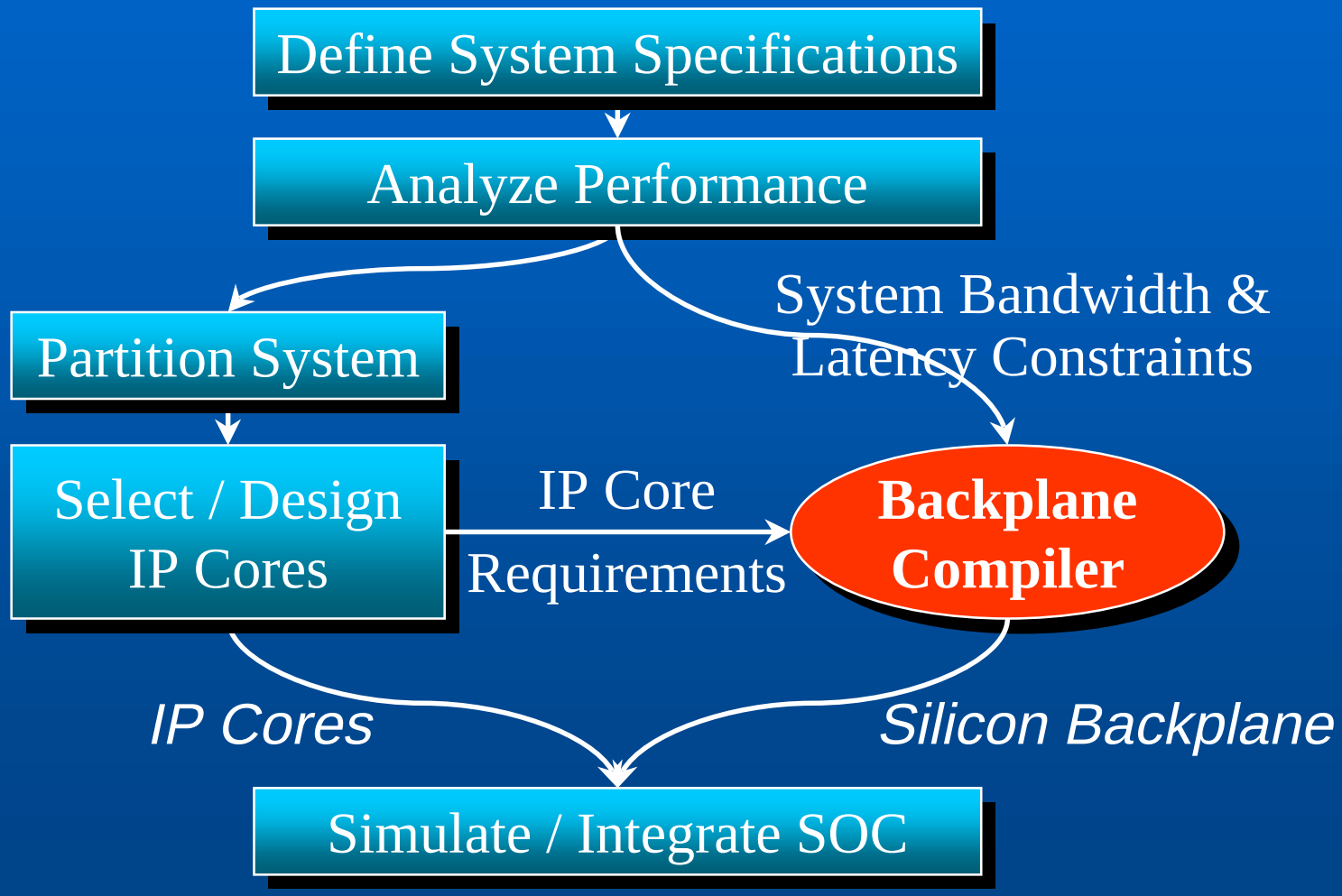
Signal	Driver	Width	Comments
Clock	Any	1	Driven by Master, Slave, or other
Cmd	Master	≤ 3	Idle, Read, Write + extensions
Addr	Master	Varies	Req. Address; VC specs width
DataOut	Master	Varies	Write Data; VC specs width
ReqAccept	Slave	1	Slave accepts request
Resp	Slave	≤ 3	Response to prior request
DataIn	Slave	Varies	Read Data; valid based on Resp
RespAccept	Master	1	Master accepts response

Simple Synchronous Read/Write Protocol with Variable Widths and Flow Control

VSIA Correspondence

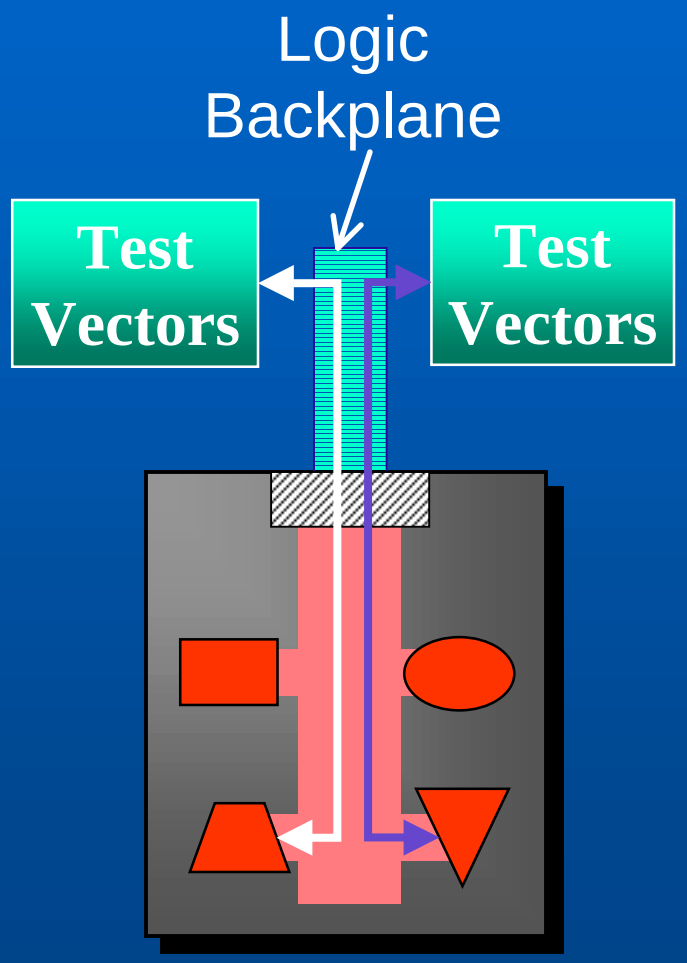


Bandwidth Engineering

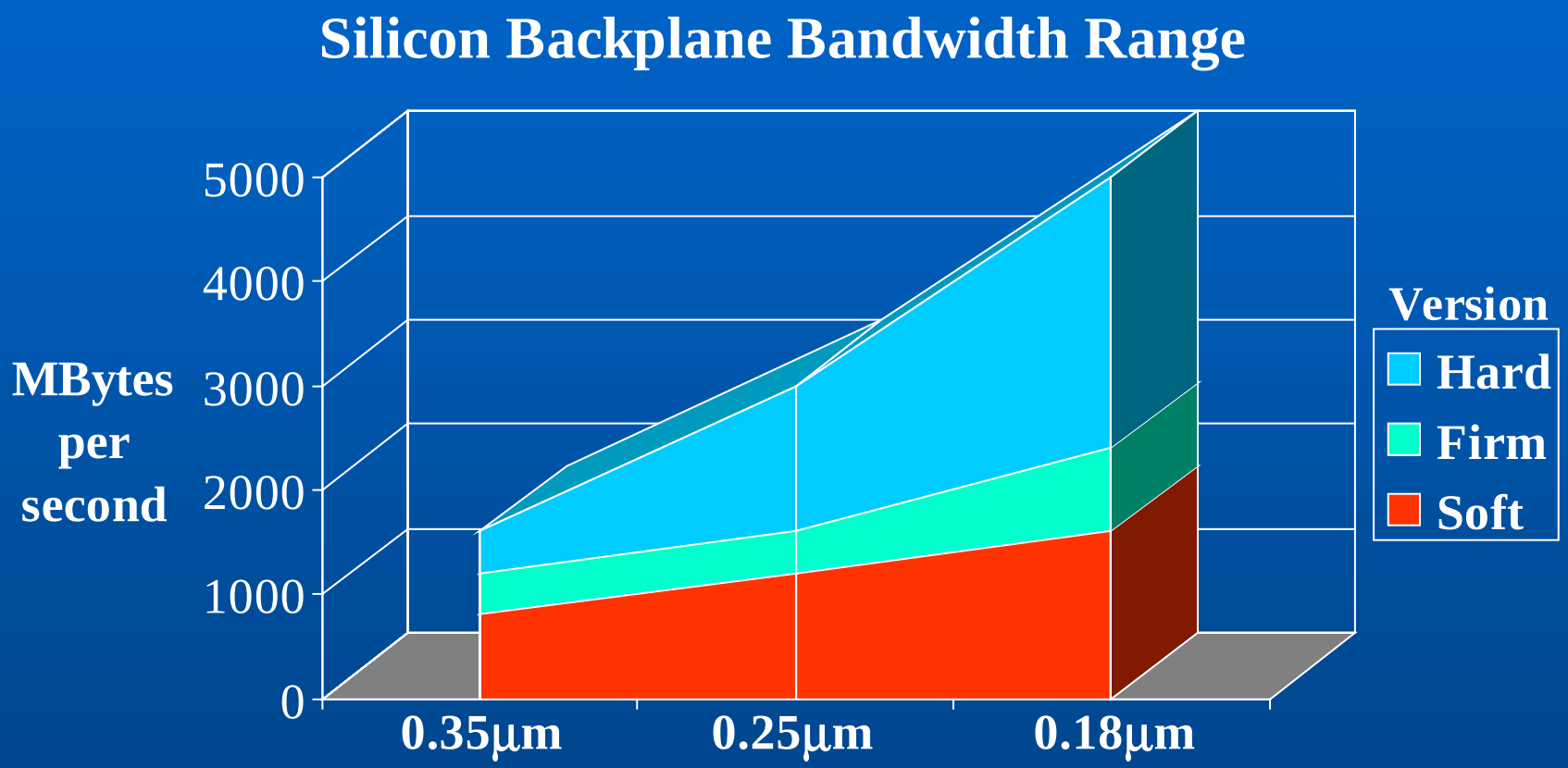


Validation / Test

- Silicon Backplane is highly visible for test
  - All subsystems communicate through Backplane
- Test Interfaces:
  - Logic Backplane: 100's MB/s
  - Snooping Module: Scan-based
- Each subsystem can be tested/validated stand-alone



Silicon Backplane Performance Roadmap



Soft and Firm versions should satisfy 90% of SOC applications

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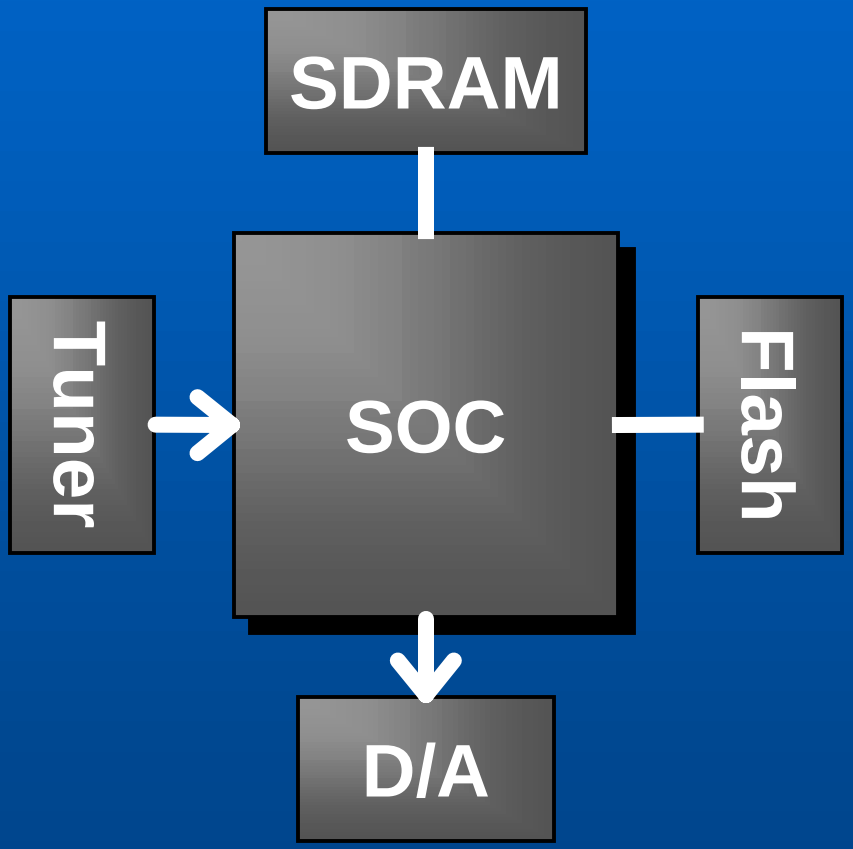
Set-top Box Application Example



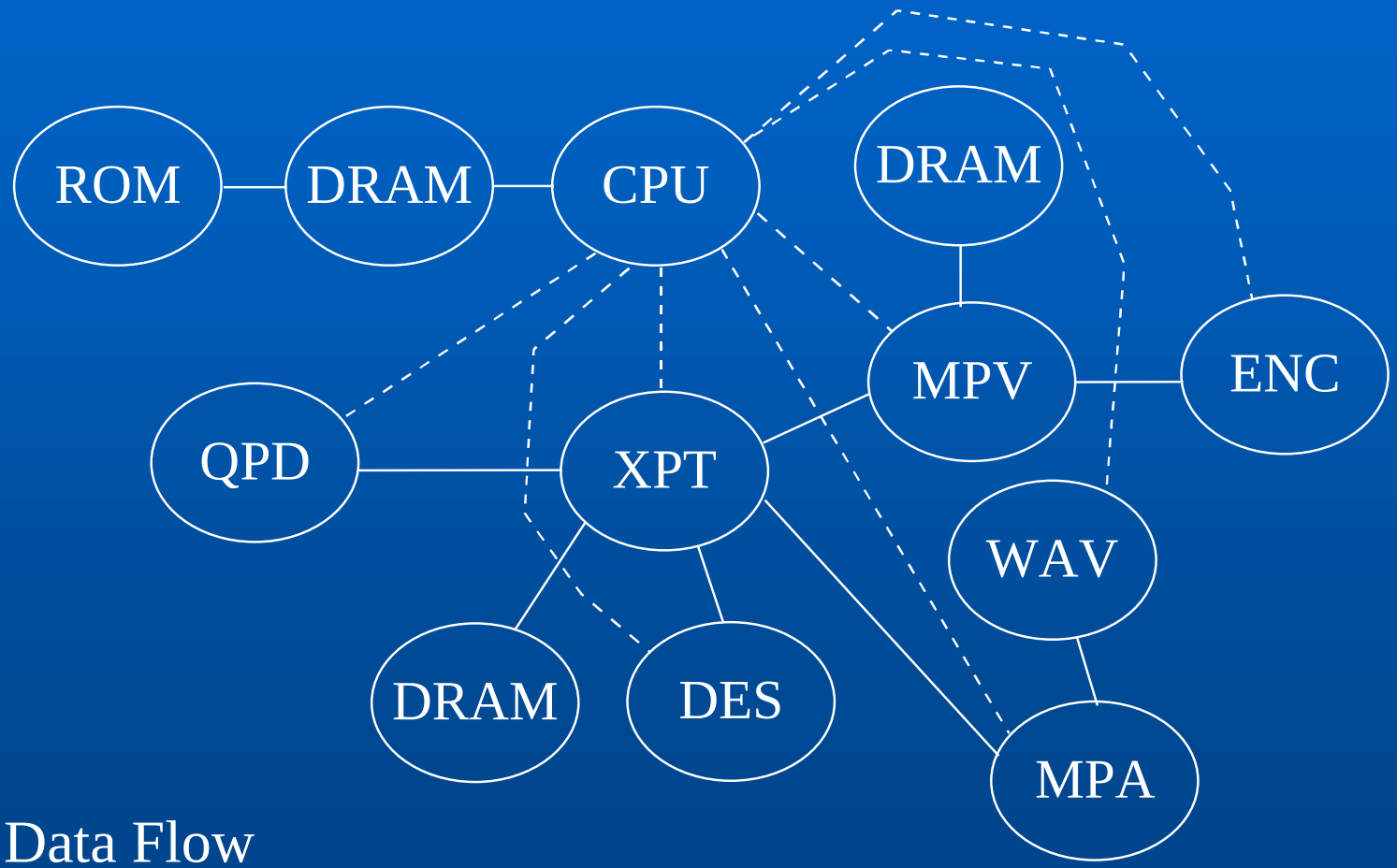
Application

- DSS set-top box with Internet browsing capability

Cores

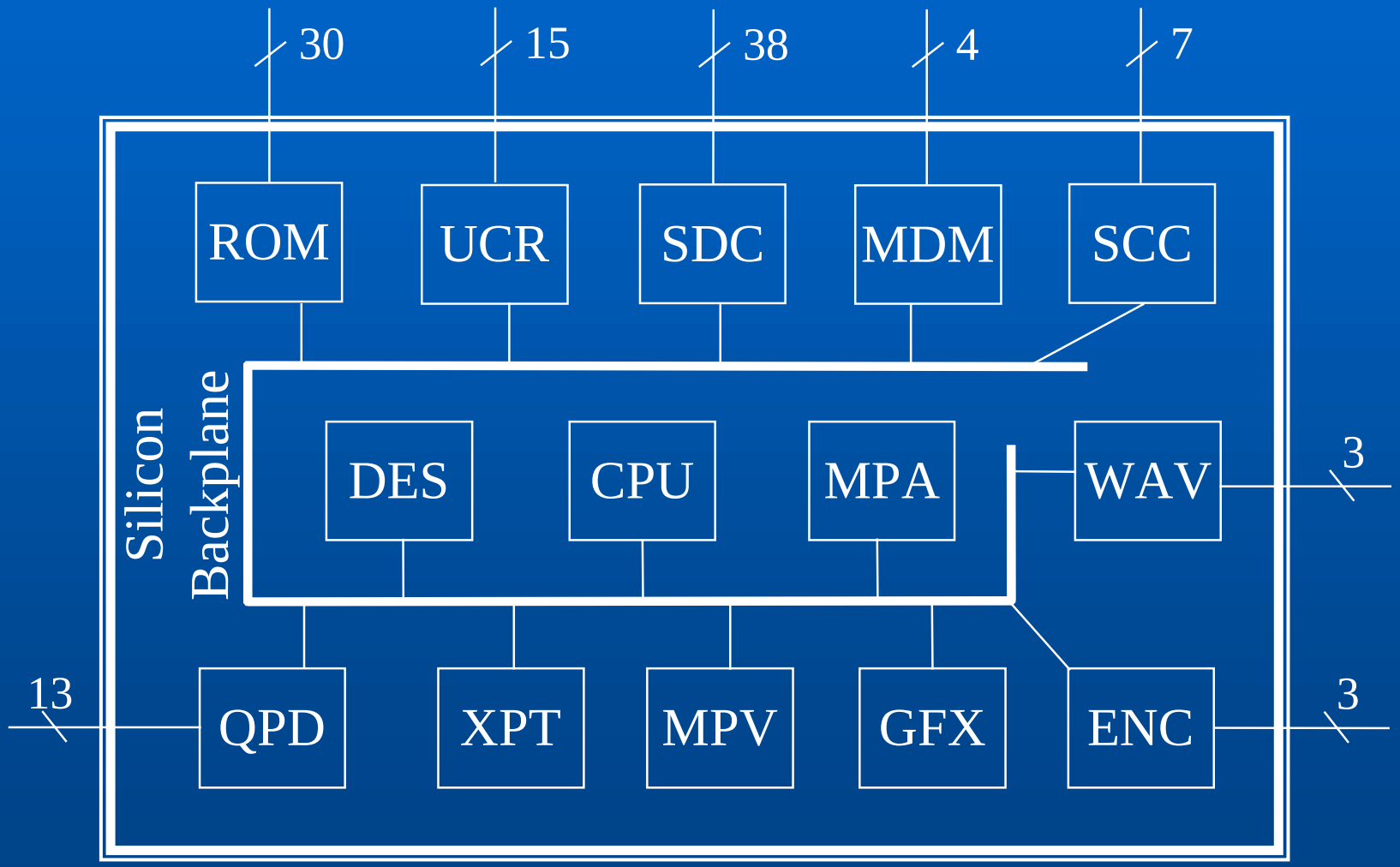
- CPU, MPEG decoder, V.34 modem, 2-D graphics, NTSC encoder, DES, SDRAM controller, Flash controller, etc.

Application Data Flow



Note: Partial Core List

Floorplan using Integration Architecture



IP Core Clock Frequencies

IP Core	MHz	IP Core	MHz
CPU	54	MDM	27
XPT	27	GFX	27
MPV	27	ENC	27
MPA	27	UCR	6.75
SDC	81	DES	6.75
ROM	6.75	WAV	27
QPD	20	SCC	6.75
Silicon Backplane	54		

64-bit Silicon Backplane @ 54 MHz → 432 MB/s

TDMA Time Slot Assignment

IP Core	Slots
CPU	114
XPT	7
MPV	28
MPA	1
WAV	1
GFX	35
Total	186 / 256 72%

Integration Architecture Benefits

- Simplifies Design
- Guarantees Performance
- Improves Efficiency
- Provides IP Plug-and-Play
- Adds Flexibility / Margin

Reduces Time-to-Market

Summary

- SOC Applications Combine Performance-Driven and Real-Time Traffic
- Proposed *Integration Architecture* Combines On-Chip, Off-Chip, and IP Core Protocols
  - Silicon Backplane and Logic Backplane Provide Configurable Bandwidth and Latency Guarantees
  - Module Interface Isolates IP Cores From SOC Application Requirements
  - Backplane Compiler Provides Simple User Interface
- Set-top Box SOC Example Demonstrates Advantages of the Architecture