EE290 A: Advanced Topics in CAD
Component Based Design of Electronic Systems
Lecture 9.2

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With contributions from Mike Keating and Prof. Ralph Ernst

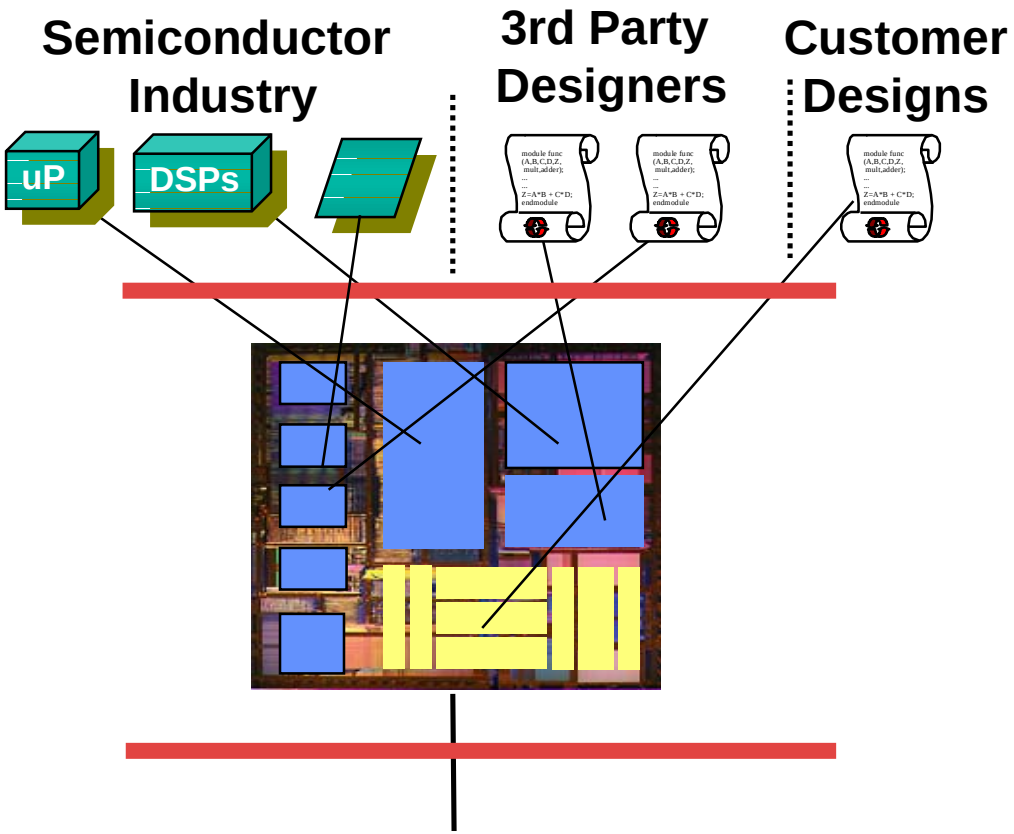
Approaches to increase IP reuse

Who is motivated to increase IP reuse?

Why do they do it?

How do they do it?

Where Does IP Come From?



Utility of Reuse - Semiconductor

Easy integration is desirable for all segments

Semiconductor industry:

- **Profits = margin_per_design X design_wins X volume_per_design**
- **High-value IP implies high margin per design**
- **currently cost of integrating a significant IP block (e.g. 32-bit risc microprocessor such as MIPS R4000) is quite high.**
- **Non-recurring engineering (NRE) cost limits volume size that can be accommodated within a particular program (>1M parts in many programs)**
- **Lower NRE costs lower the barriers to utilizing semiconductor IP. More design_wins means more volume. More volume means more profit.**
- **Semiconductor companies are also trying to glue customers into their fab**

Utility of Reuse - 3rd party IP

Easy integration is desirable for all segments

3rd party IP:

- **Profits = fixed_charge_per_design X design_wins + (royalty)**
- **royalty = royalty_per_design X design_volume**
- **Since principle source of revenue comes from fixed charges per design, 3rd party IP companies are more highly dependent on design wins than are semiconductor companies, thus they are even more motivated to make integration easy.**
- **Lower NRE costs lower the barriers to utilizing 3rd party IP. More design_wins means more fixed charges. More charges, more profit.**

Utility of Reuse - Customer designs

Easy integration is desirable for all segments

Customer designs:

- **Focus is on reducing NRE costs for design an integrated circuit**
- **Lower NRE costs lower the barriers to utilizing 3rd party and semiconductor IP and reduces overall design cost**
- **In addition, while semiconductor companies wish to use high-value IP (e.g. TMS320CXX) to tie end customers to a fab. End customers, on the other hand, desire NOT to be tied to a particular semiconductor fabrication facility. Variety of IP designs as well as variety of access is desirable.**

Summary of Motivation

Across the board, the market forces motivate:

- **Providing a wide variety of intellectual property blocks**
- **In a manner that makes it easy to integrate the IP blocks**

OK, so how do we do it?

Technical Challenges to Integration

Verification

- **Functionality**
- **Electrical correctness**
- **Testability**

Performance parameters

- **Timing**
- **Power**
- **Area**

How the integration challenge is faced

Semiconductor company

- **Motorola CSIC program - MC68332**
- **LSI Logic Coreware program**
- **(TI - cDSP - custom DSP Program)**

3rd party IP provider

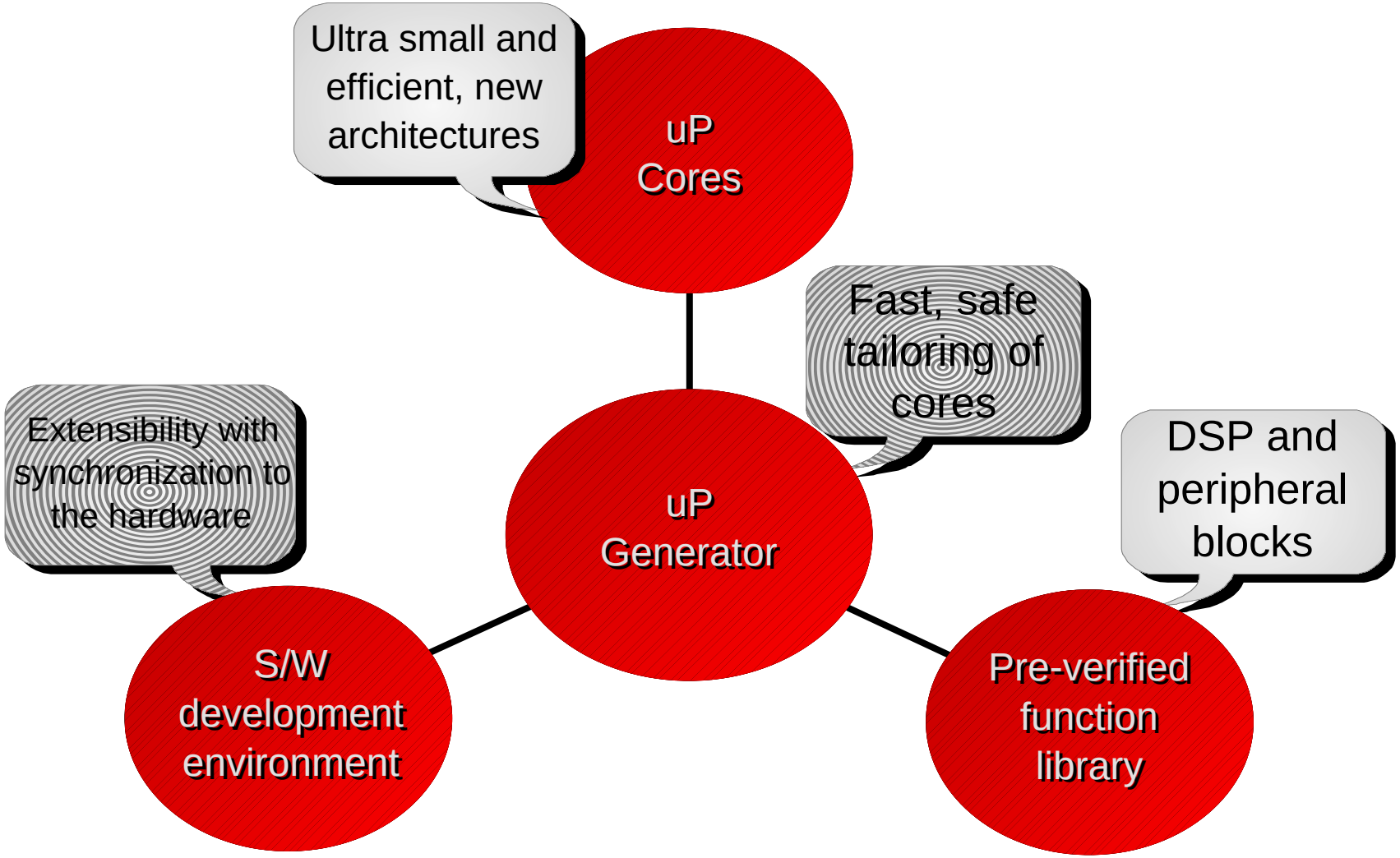
- **(Inventra)**
- **Tensilica Xtensa Processor**
- **Synopsys 8051**
- **Sonics (auxillary slides)**

End Customer

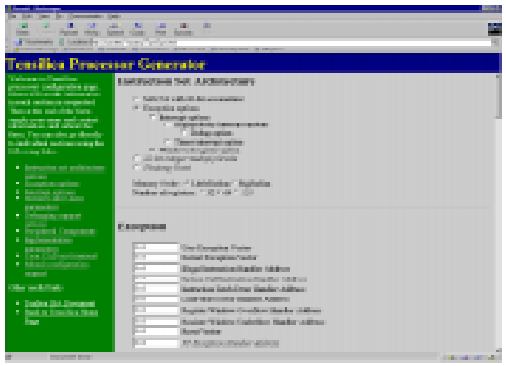
- **Reuse methodology consulting**

Third Party IP Suppliers

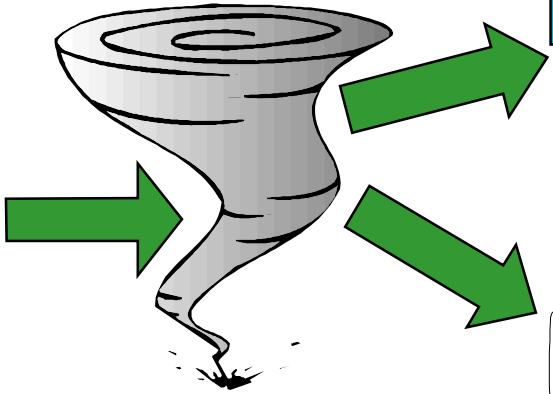
The tensilica solution:



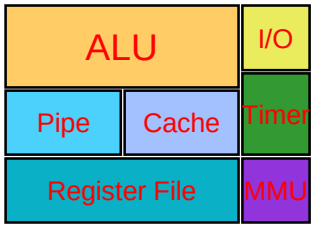
Imagine the possibilities……



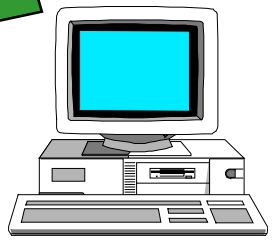
Describe the processor attributes from a browser-like interface



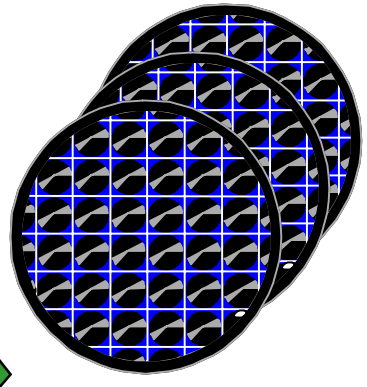
Using the ***tensilica*** processor generator, create...

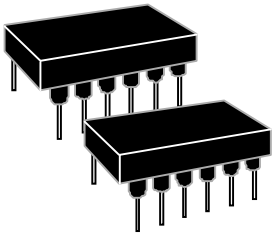


Tailored, RTL uP core



Customized Compiler, Assembler, Linker, Debugger, Simulator

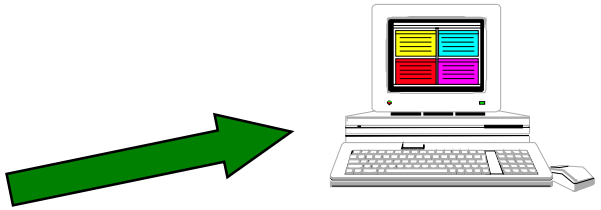




Use a standard cell library to target to the silicon process

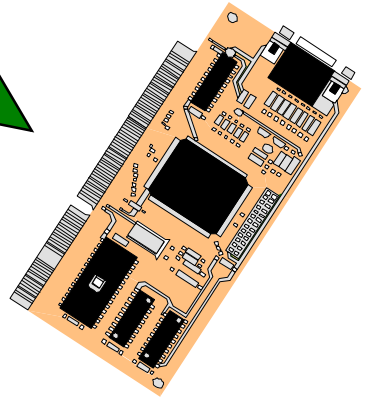
Prototype and Emulation Support

- Uniform interface to a robust co-verification suite



Cycle Accurate
Instruction Set Simulator

Verilog
VHDL



FPGA-based HW emulator

Standard EDA tools are supported

Function	EDA Tool Support
Logic Synthesis	Synopsys, Ambit
Logic Simulation	Verilog XL/NC, VCS, MTI, Vantage
Timing Analysis	MOTIVE, Primetime, PEARL
Floorplanner	HLD
Place/Route	Si Ensemble, Apollo, Aquarius
LVS/DRC	DRACULA

DW8051 : The Complete Solution

Creation

Synopsys

"Embedded System On A Chip" Design Flow

Evaluation → Development → Simulation → Synthesis → Fabrication → System Debug

HardWare Development

DW8051 Source Code
- VHDL Source
- Verilog Source
- 8031/8032
- 8051/8052

Multi-Simulators Tested/Supported
- VSS
- Vantage
- MTI
- Leapfrog
- Verilog-XL
- Chronologic

Synthesis Support
- Syn. Scripts
- Test Compiler
  Scan Insert
  98% Fault Cov.

Technologies Tested/Ported
- 0.6Micron CBA Silicon
- 0.6Micron TSMC CBA
- 0.6Micron Charter CBA
- 0.65Micron LSI300K
- 0.5Micron LSI500K
- 0.5Micron Motorola H5C
- 0.5Micron Oki

DW8051 Evaluation Kit
- DW8051 CBA Si
- DW8051 Daughter Card
- Keil 8051 Eval Kit
  - Keil Eval Board
  - C Compiler
  - 8051 Assembler
  - Debug Software

Complete System Debug & Development Environment Tested
- Hitex In Circuit-Emulator
- ChipView Software Debugger
- Multiple C-Compilers Tested
- 8051 Assembers Tested

SoftWare Development

Software Development Tools
- DW8051 CBA Silicon
- DW8051 Daughter Card
- ChipView-51 Software Debugger

From Start to Finish
We Provide Designers
The Complete Solution!!!

Design for Reuse

Synopsys

- General Solution
  - parameterized for various applications
- Meets quality goals in multiple technologies
- Designed to simulate with common commercial simulators (Verilog and VHDL)
- Fully Verified
  - reuse requires higher confidence levels - 99%
  - complete test bench for system integration

Why Reuse is Hard

Synopsys

Requires best design practices

Requires generalized solutions

Verification of parameterized designs is hard

Optimal, generalized synthesis is hard

Requires

- discipline
- processes
- tools
- additional effort and time
- management buy-in that value >> cost

High Quality Documentation

Synopsys

1st Generation

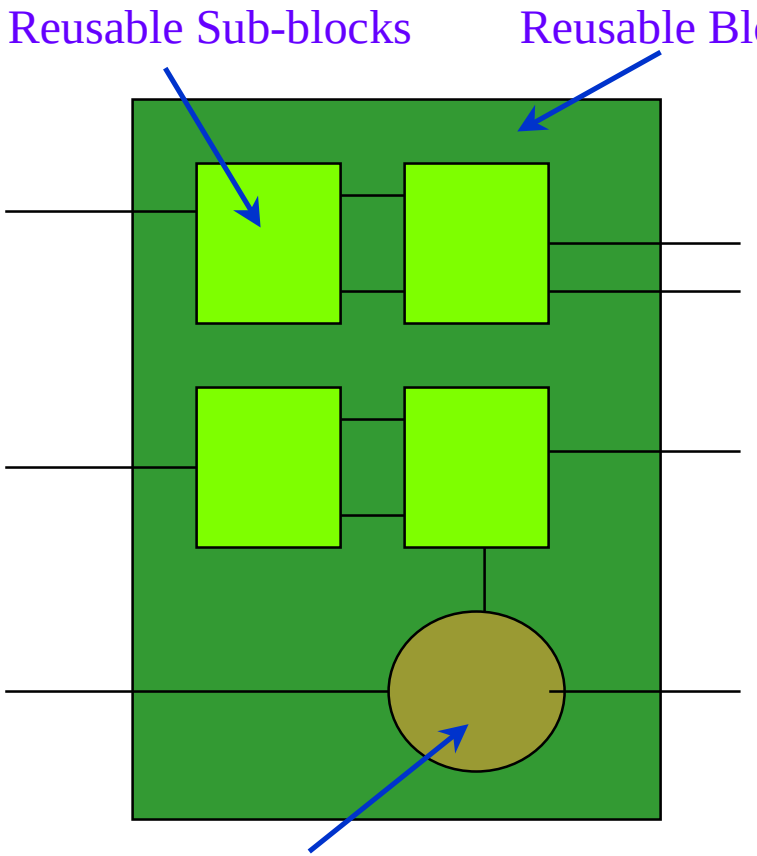
- Block Diagrams
- Functional Specification
- Description of parameters
- Interface signal description
- Timing diagrams/req'ments
- Verification Strategy
- Synthesis Constraints

1st Thru nth Generation

- Project it was used on
- Personnel on the project
- Verification Report
- Technology used
- Tools (w/version) used
- Actual Timing/Area Results
- Revision history for any modifications

Example of Poor Partitioning

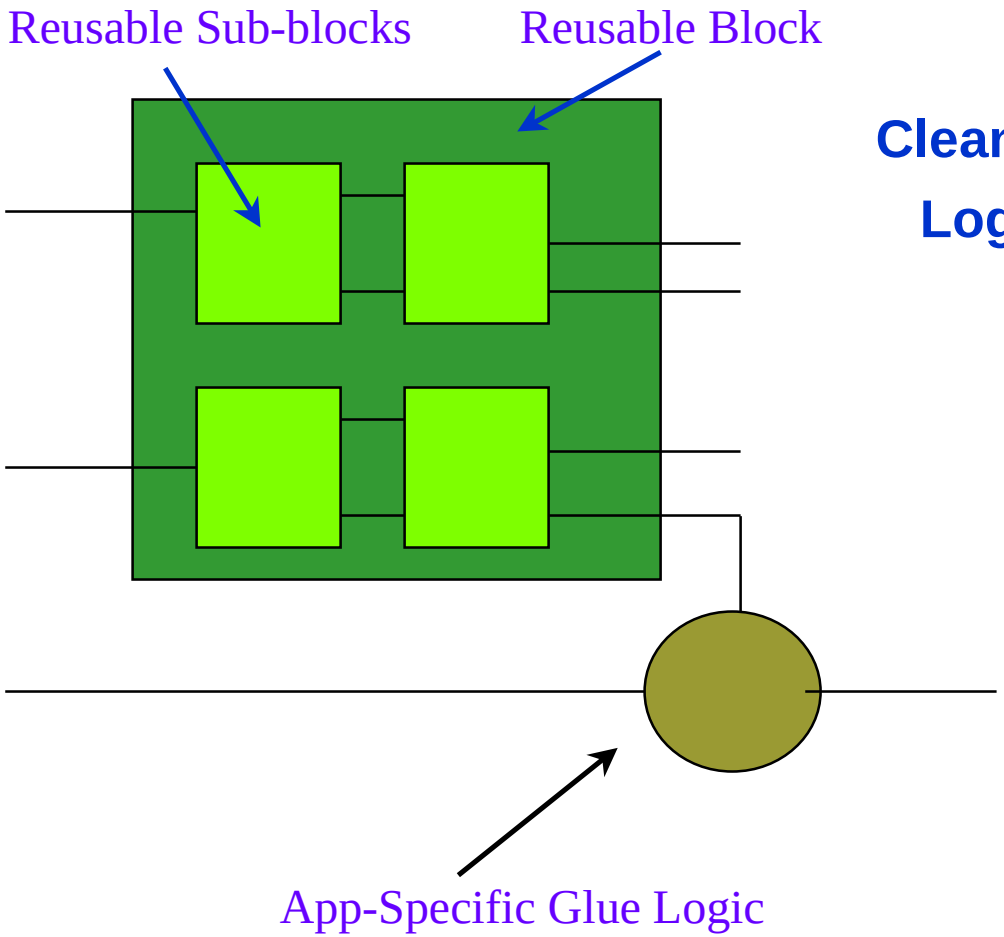
Synopsys



Separate Application-Specific Logic from Reusable Sections

Example of Good Partitioning

Synopsys



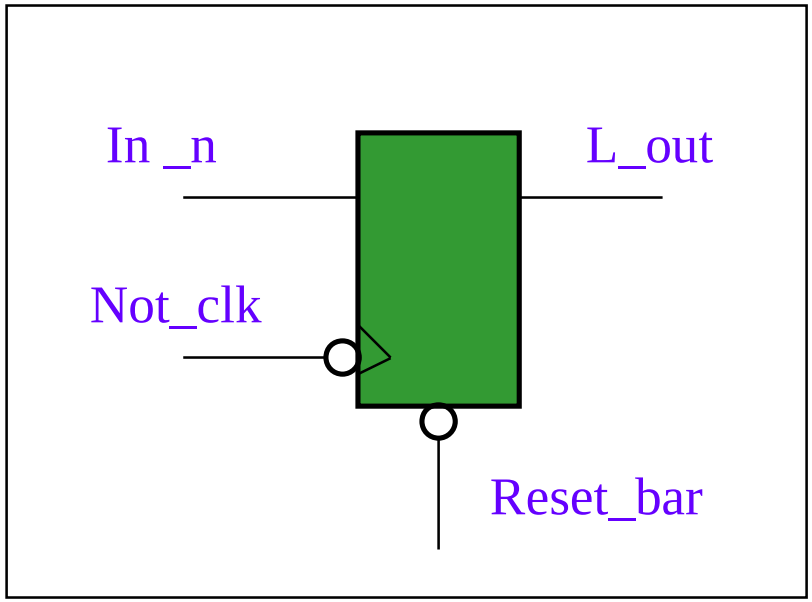
Clean Partitioning of Glue Logic Away from Main Reusable Areas

Consistent Coding Guidelines are Key

- Signal Naming Conventions
- Blocking vs Non-blocking ops
- Signals vs variables (VHDL)
- Sync vs Async resets
- Copyright banners
- Change history
- Indentation
- Begin/End closure
- Commenting do's/don'ts
- Use of constants/defines
- Design for test constructs
- State machine coding
- Technology portability

Synopsys

4 of many ways to name active low signals. Pick one!

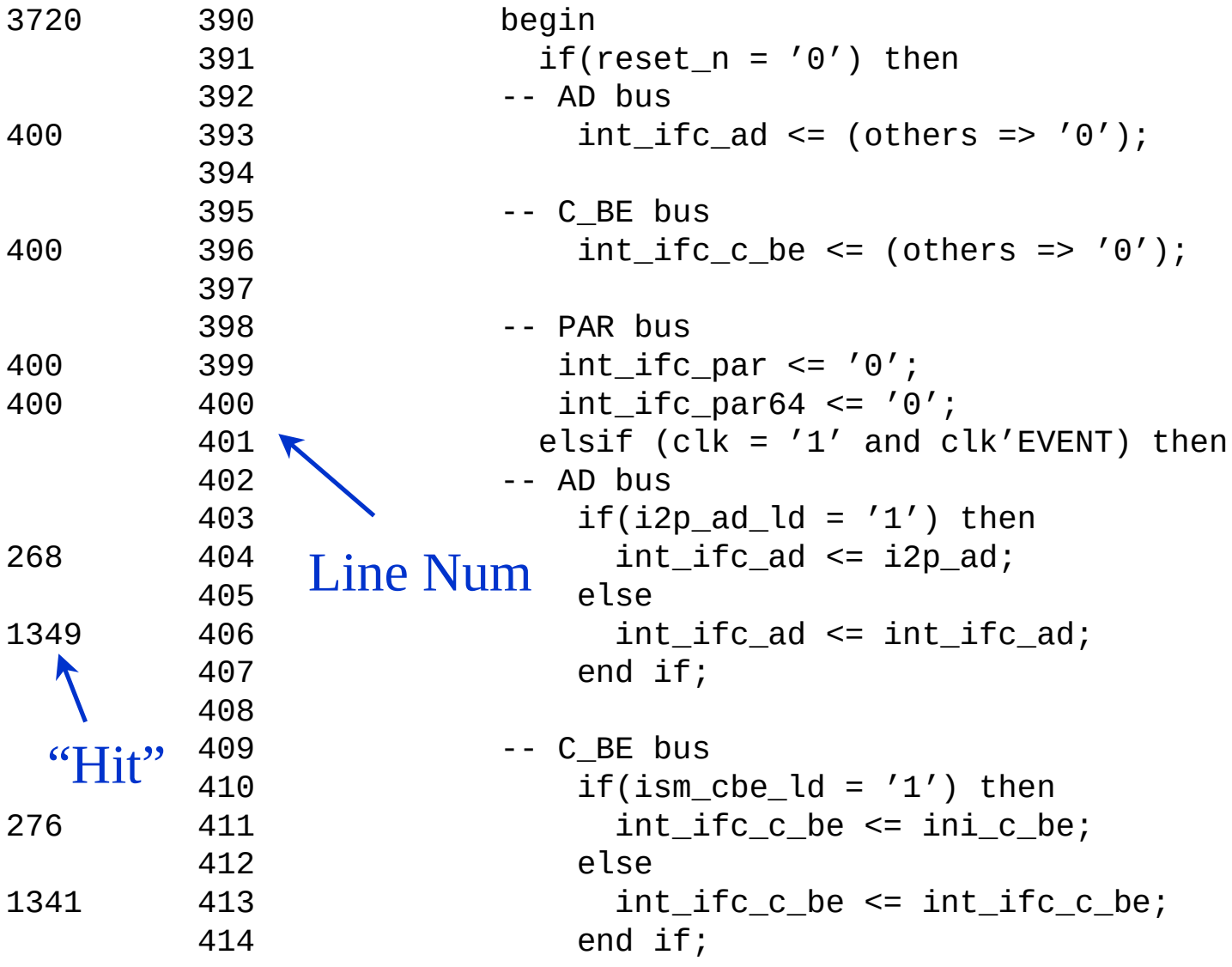


Verification is Key to Reuse

Synopsys

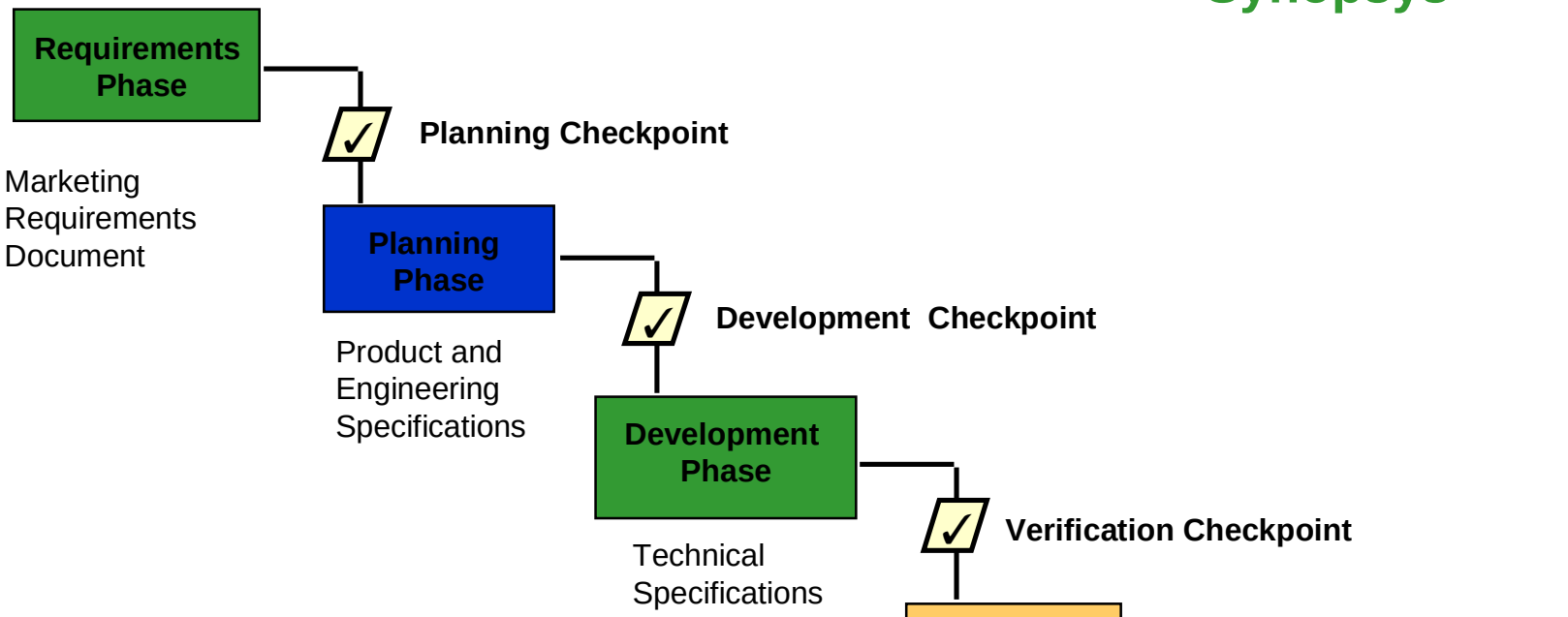
Code Coverage Reports

Synopsys



DesignWare™ Development Lifecycle

Synopsys

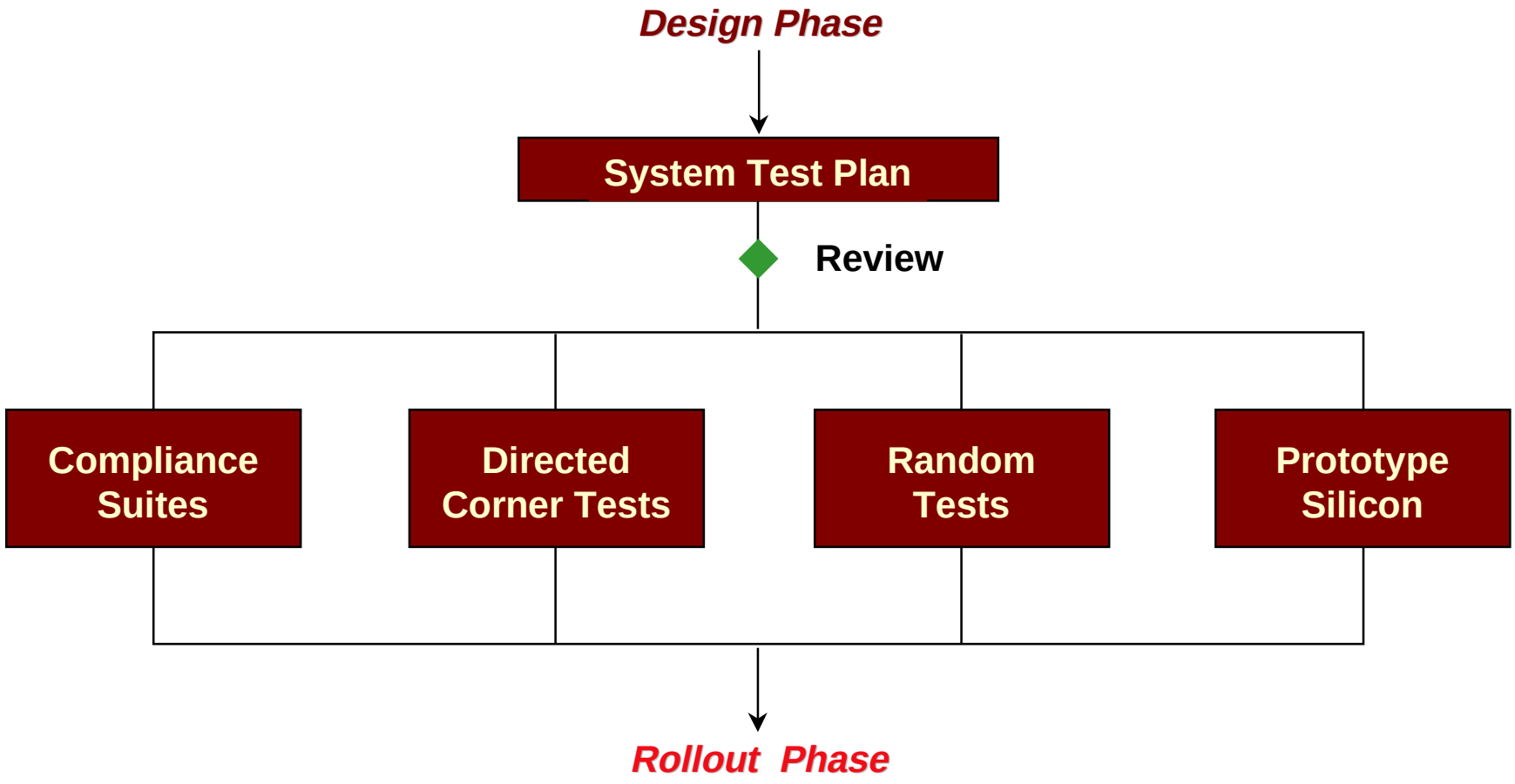


All blocks adhere to common process

- ✓ Strict pass criteria at each checkpoint
- ✓ Signoff required for each phase
- ✓ ISO 9000-like

Verification Phase Activities

Synopsys



Semiconductor Companies

Example: Motorola MC 683xx - family of controllers

Processor: CPU 32

- **68000 - processor enhanced by most of the 68030 features**
- **CISC processor: code density**
- **pipelining**
- **standard register sets (not in RAM)**
  ⇒ context switch is more expensive
- **virtual memory**
- **supervisor and user modes**

} **aims at use of operating systems**

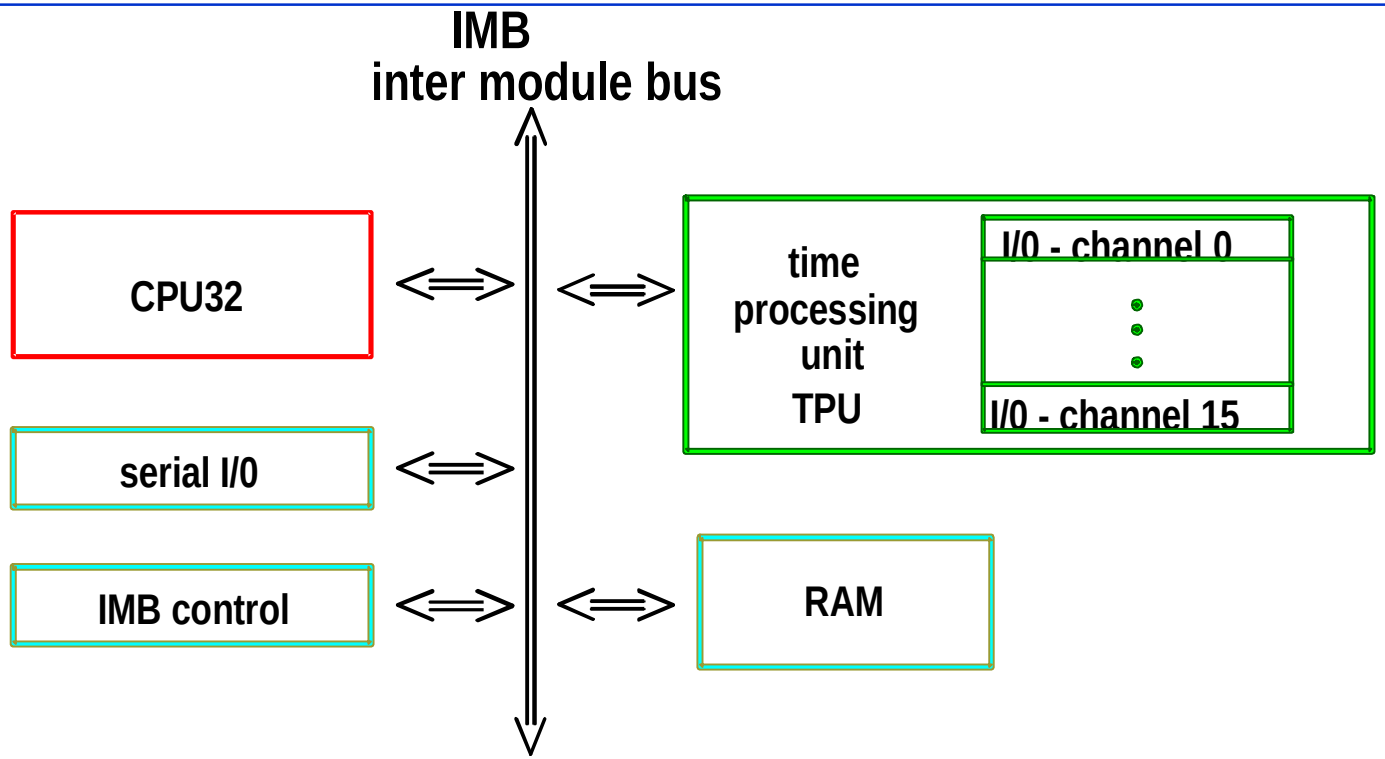
- table lookup instructions for compressed tables with built-in linear interpolation
  ⇒ data density is concern

http://motorola.com/SPS/MCU/lit/manuals/332um/outline1.html

control dominated systems

Source: Prof. Rolf Ernst

MC68332



Designed for automotive applications with mixture of computation intensive tasks and complex I/0 -functions

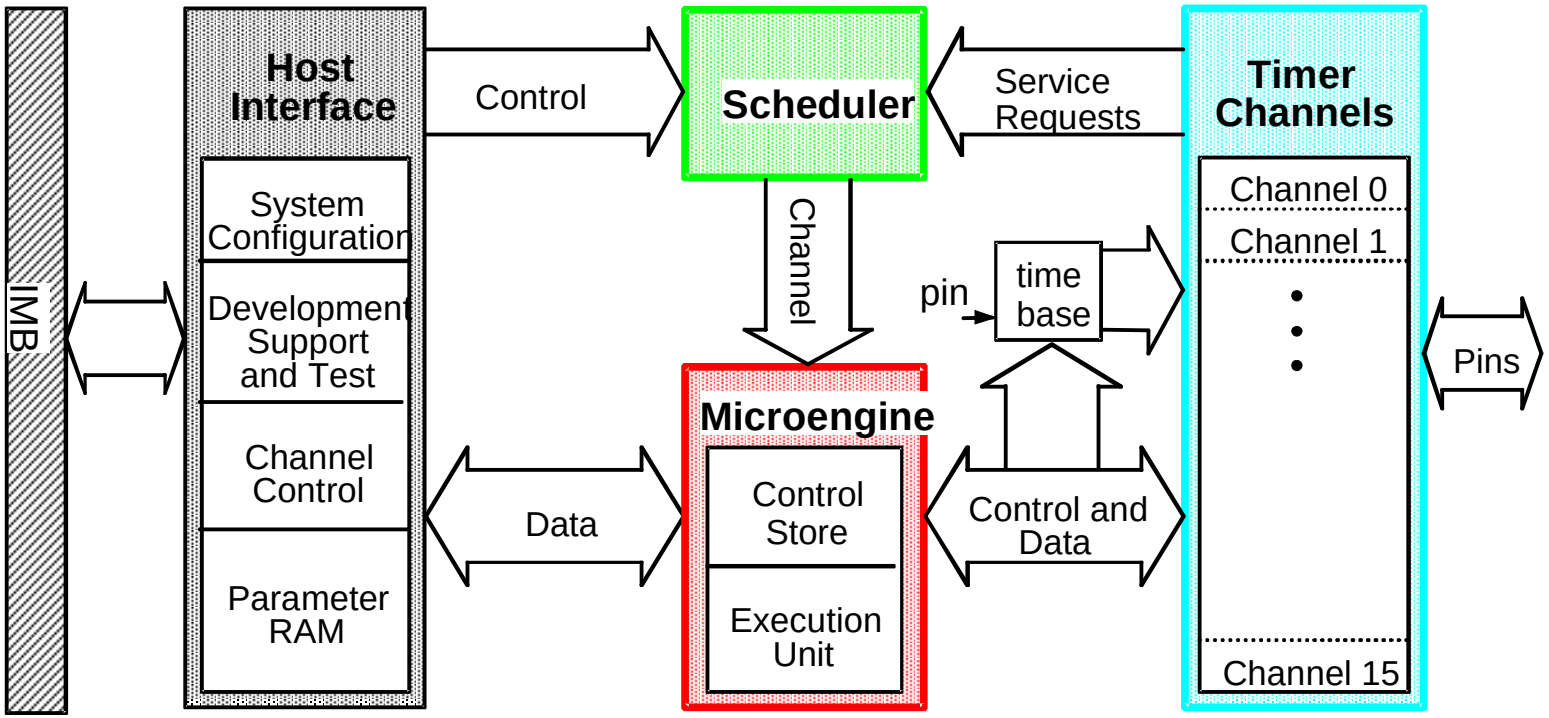
Idea: off-load CPU from frequent I/0 interactions to make use of computation performance: ⇒ TPU

control dominated systems

Source: Prof. Rolf Ernst

MC68332

- independent programmable timer channels: single-shot "capture & compare"
- channel coupling and sequence control with control processor



TPU: time processing unit: peripheral coprocessor

control dominated systems

Source: Prof. Rolf Ernst

http://www.lsil.com/products/unit5_5.html

A Sample of LSI Logic's CoreWare Core Availability	Product Family 300K	500K	60XK	G10™	G11™
TinyRISC 16/32-bit Embedded TR4101 CPU				A	
TinyRISC 16/32-bit Embedded TR4102 CPU Embedded in Easy MACRO (EZ4102)					P
MiniRISC 32-bit Superscalar Embedded CW4003 CPU				A	
MiniRISC 32-bit Superscalar Embedded CW4011 CPU				A	
MiniRISC 64-bit Embedded CW40XX CPU				P	P
OakDSPCore CPU 16-bit Fixed-Point CWDSP1640		A			
OakDSPCore CPU 16-bit Fixed-Point CWDSP1650				A	
GigaBlaze Transceiver				A	P
Merlin Fibre Channel Protocol Controller		A		P	
Viterbi Decoder		A			
Reed-Solomon Decoder		A(DBS)			
Ethernet-10 Controller (Incl. 8-wire TP-PMD), 10 Mbps	A		A		
MENDEC-10 Ethernet Manchester Encoder-Decoder, 10 Mbps			C		
Ethernet-110 MAC, 10/100 Mbps	A	A	A		
SONET/SDH Interface (SSI) 155/51 Mbps	A	A	A		
ARM7 Thumb Processor				A	
T1 Framer			A		A
HDLC				A	
Ethernet-110 Serdes, 10/100 Mbps	A	A	A		
Ethernet-110 100BASE-X, 10/100 Mbps	A	A	A		
PHY-110, Ethernet Auto Negotiation 10/1000 Mbps			Q2-98		
USB Function Core				A	Q2-98
PCI-66 FlexCore™ Core				A	A

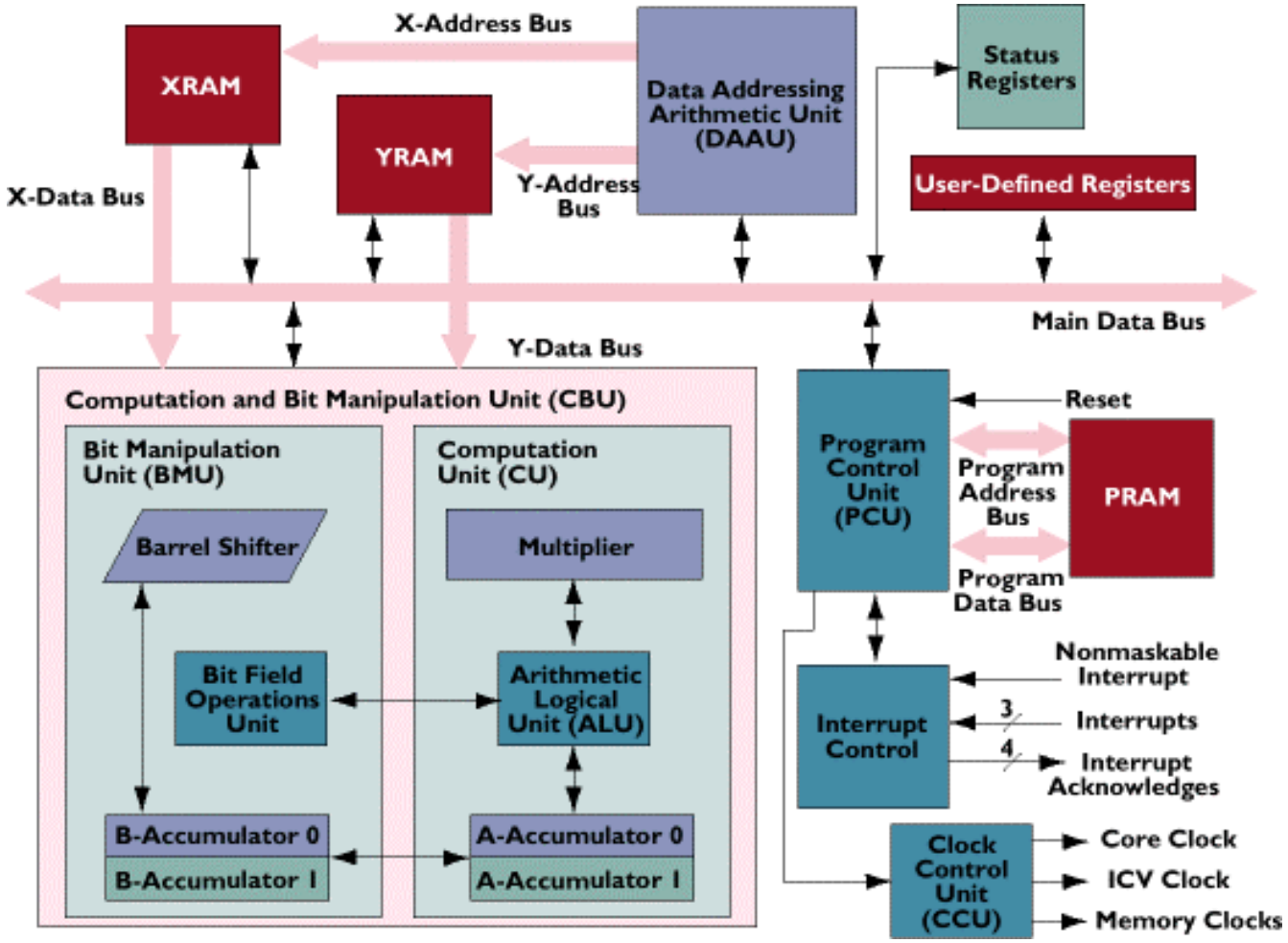
For a listing of additional cores, contact your local LSI Logic sales representative.

A = Available C = Consult Marketing P = Planned Technology

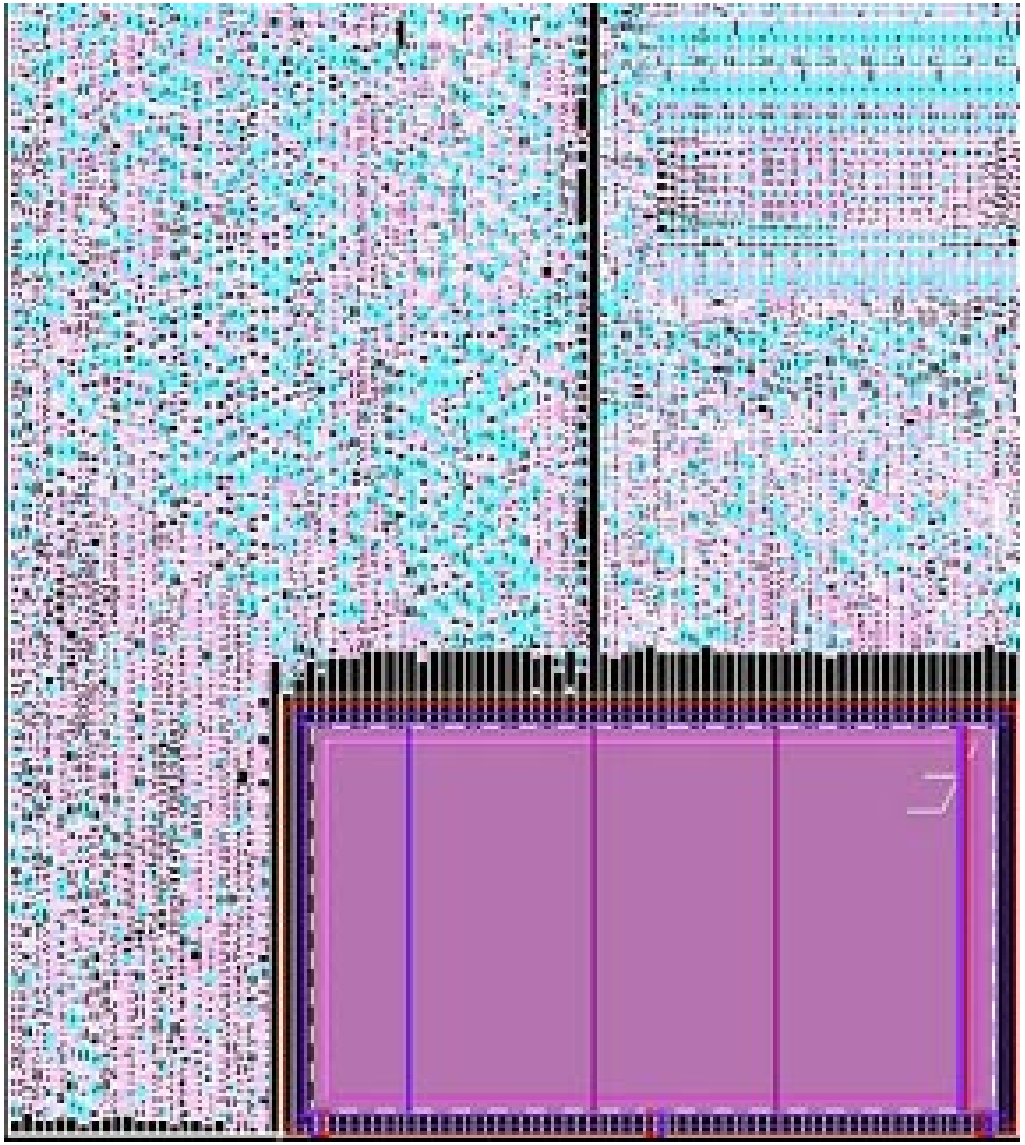
A Sample of Mixed Signal Cores	Product Family LCB500K	LCB60XK	G10 Products	G11 Products
1-bit Slicer ADC 10 MSPS	√		√	
4-bit Low Power Flash DC 10 MSPS	√		√	
6-bit Flash ADC 60 MSPS	√			
6-bit Flash ADC 90 MSPS			√	
8-bit Flash ADC 40 MSPS	√		√	
10-bit Successive Approximation ADC 350 KSPS	√		√	
Triple 10-bit RGB Video DAC	√	√	√	√
10-bit Low Power DAC 10 MSPS	√		√	
10-bit Low Power Multiple Output DAC	√		√	
Sample and Hold Output Stage for 10-bit Low Power Multiple Output DAC	√		√	
Programmable Frequency Synthesizer 300 MHz	√		√	
SONET/ATM 155 MSPS PMD Transceiver	√			
155 and 207 MBPS High Speed Backplane Transceiver	√			
Ethernet 10BASE-T/AUI 4/6 Pin, 5 V		√		
Ethernet 100BASE-X Clock Generation/Data Recovery Function, 3 V		√		

Note: Most of the mixed signal cores listed above will be ported to the G11 product family. Contact your local sales representative for schedule information.

OakDSPCore CWDSP1650



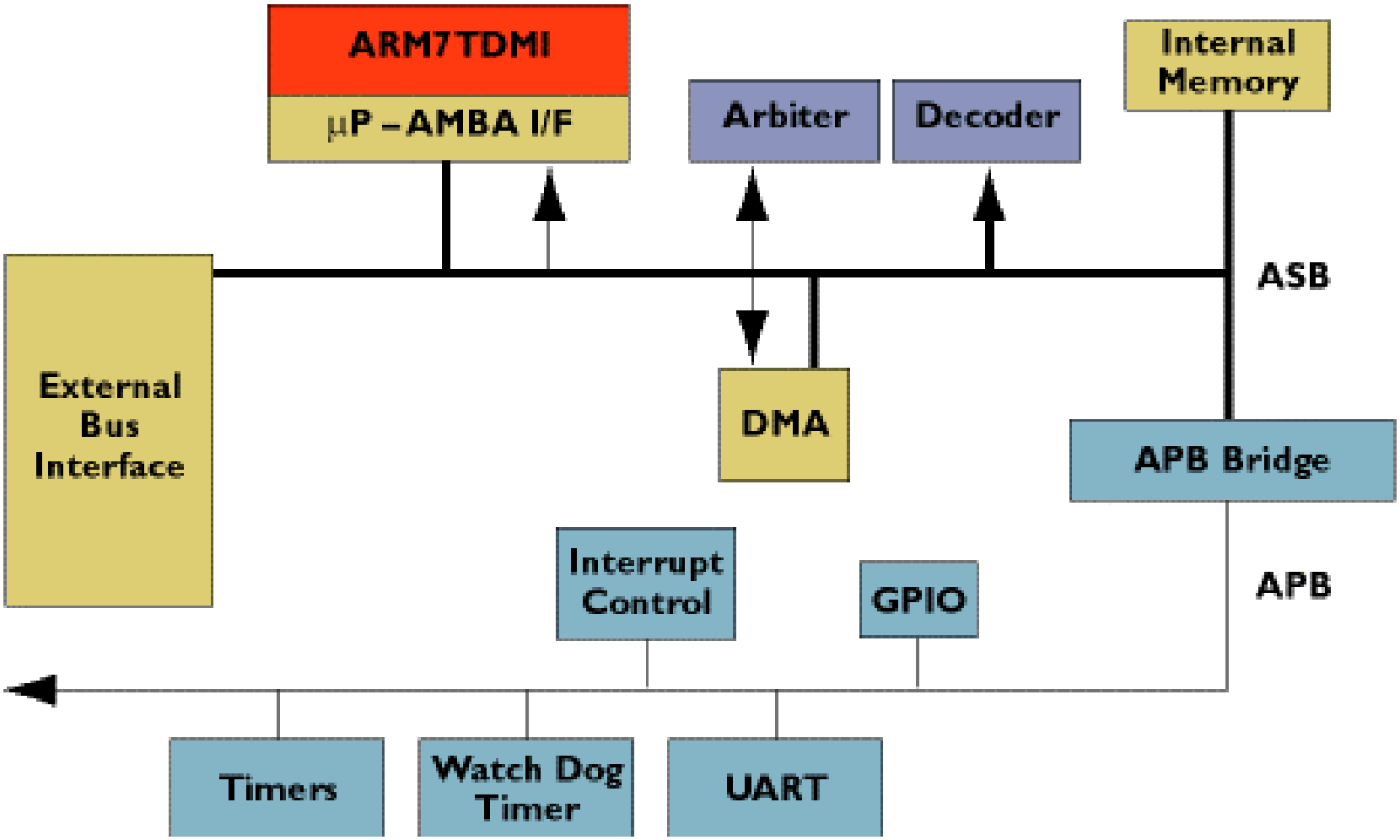
ARM Core7 Thumb Embedded



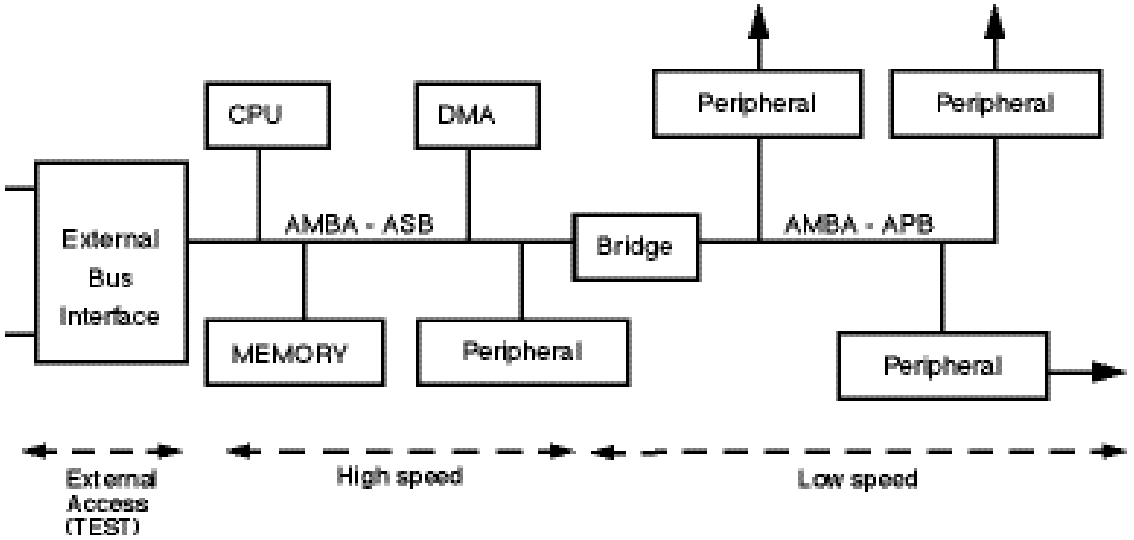
ARM/LSI's Features to Ease Integration

- ***synthesizable*** **version of the widely popular ARM7TDMI processor core**
- **''LSI Logic's RTL-level approach, implemented with the CoreWare design methodology, results in the fastest time-to-market for system-level ASICs in the industry. ''**
- **''LSI Logic's ARM cores are also supported with a rich set of peripherals easing the implementation of a complete CPU subsystem in a large system-level ASIC. This peripheral library, including complex peripherals like SDRAM controllers, is constructed around the open AMBA standard facilitating IP reuse.''**
- **''These building blocks have been designed to facilitate customization to specific requirements.''**

ARM7 core


ARM7TDMI
μP – AMBA I/F
Arbiter
Decoder
Internal Memory
ASB
External Bus Interface
DMA
APB Bridge
Interrupt Control
GPIO
APB
Timers
Watch Dog Timer
UART

ARM's Amba open standard



Advanced System Bus, (ASB) - high performance, CPU, DMA, external

Advanced Peripheral Bus, (APB) - low speed, low power, parallel I/O, UART's

External interface

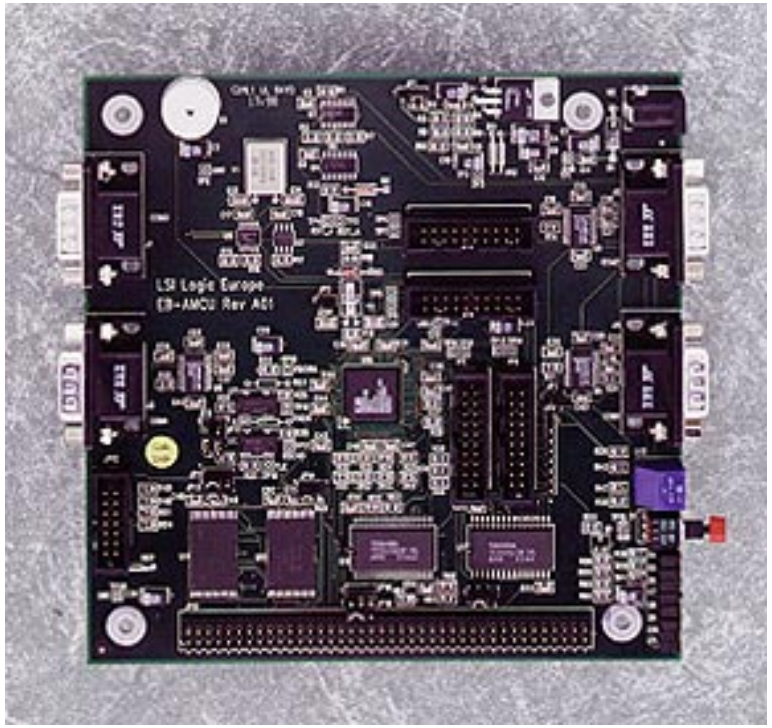
http://www.arm.com/Documentation/Overviews/AMBA_Intro/#intro

More Features to Ease Integration

- **LSI Logic's ARM cores are supported with the ARM software development toolkit.**
- **This integrated development environment, available on multiple hosts, comes with the full ARM compiler suite and complete debugging environment including**
- **the ARMulator, cycle accurate instruction set simulator, which supports simulation in an off-line mode or can be connected via a JTAG port to the target application for real time debugging even in large, complex ASICs.**

Even more Features to Ease Integration

The development software is complemented with the standard PID7T H/W evaluation board provided by ARM or LSI Logic's AMCU development board which features a highly integrated MCU show casing the peripherals available in the library.



End Customer Integration

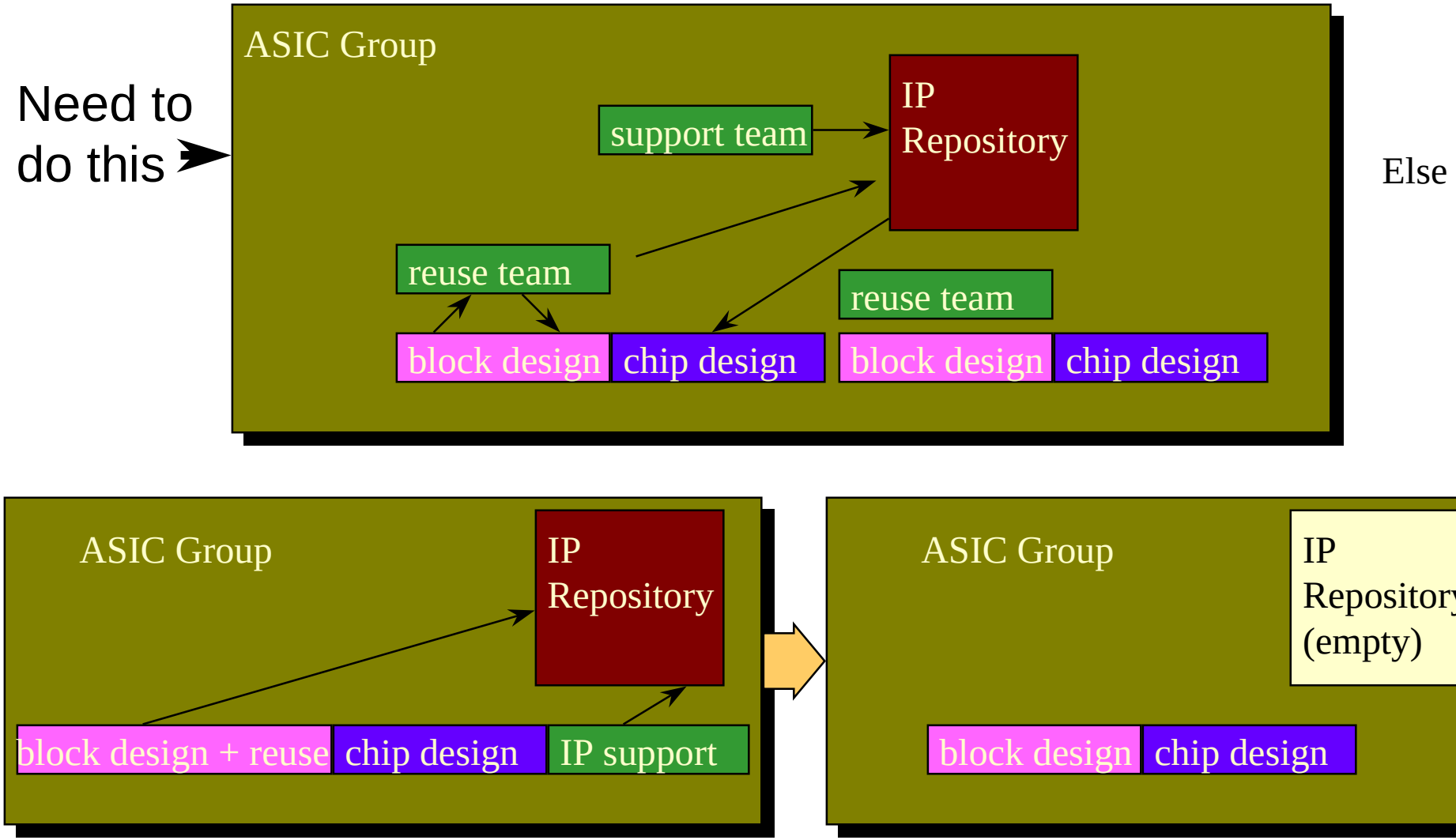
Who will "manage" your Internal IP?

An effective strategy requires some degree of internal coordination

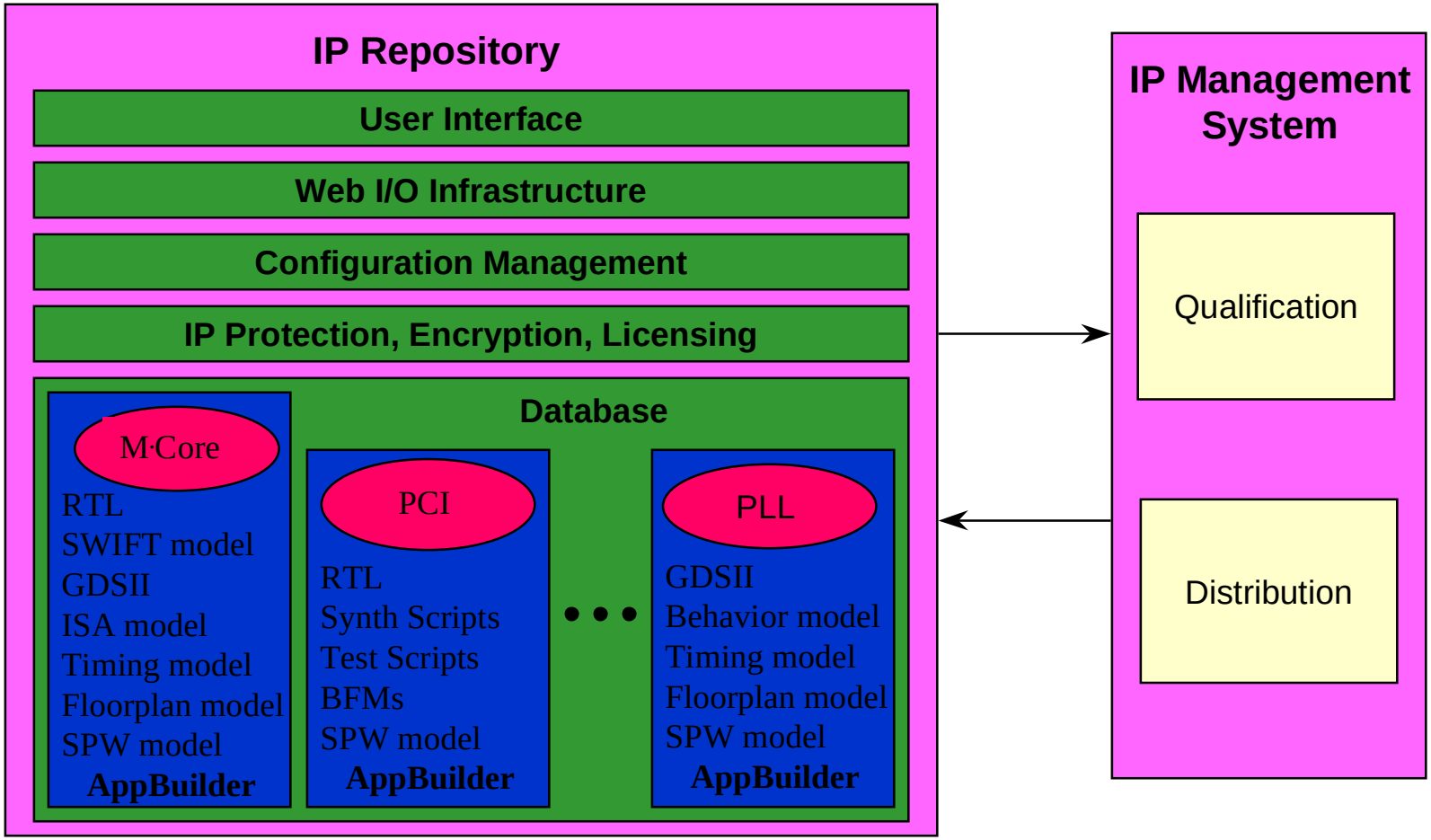
Some possibilities:

- **R&D group**
- **CAD group**
- **Document Control group**
- **Quality group**

Organizing for Reuse-Based Design



IP Repository -
Heart of the EcoSystem Infrastructure



Summary

All segments are motivated to increase design reuse

- 3rd party IP supplier
- Semiconductor
- End system customer

Approaches to increasing reuse

- Increasing breadth of capability
- Increasing ease of integration
  - easy to verify function
  - easy to verify timing
  - easy to verify electrically
- generally, easy to integrate in tool flow