System-on-a-Chip and Interfaces

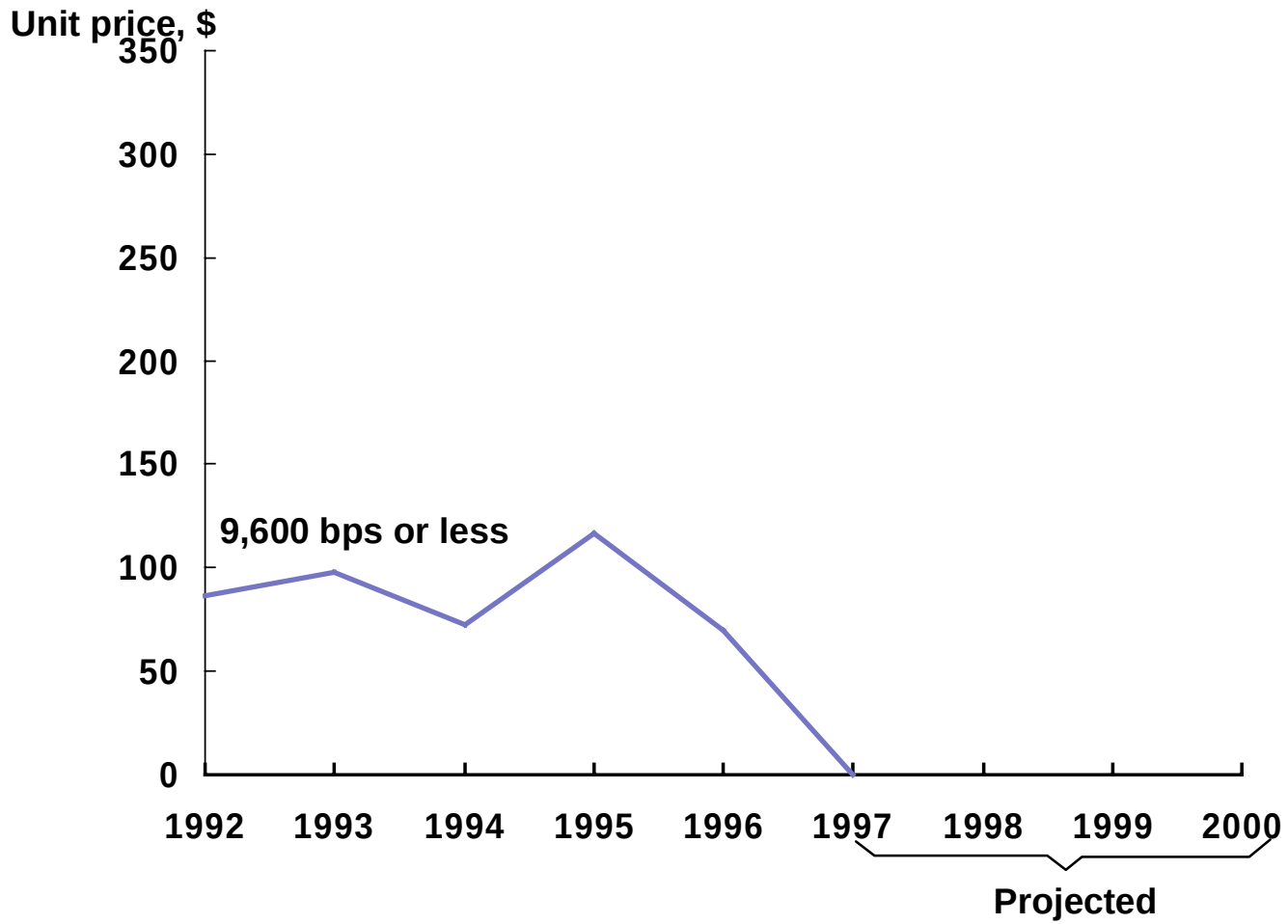
Richard Newton

University of California at Berkeley

Framework in Which to Understand System on a Chip

IMPACT OF SUBSTITUTION

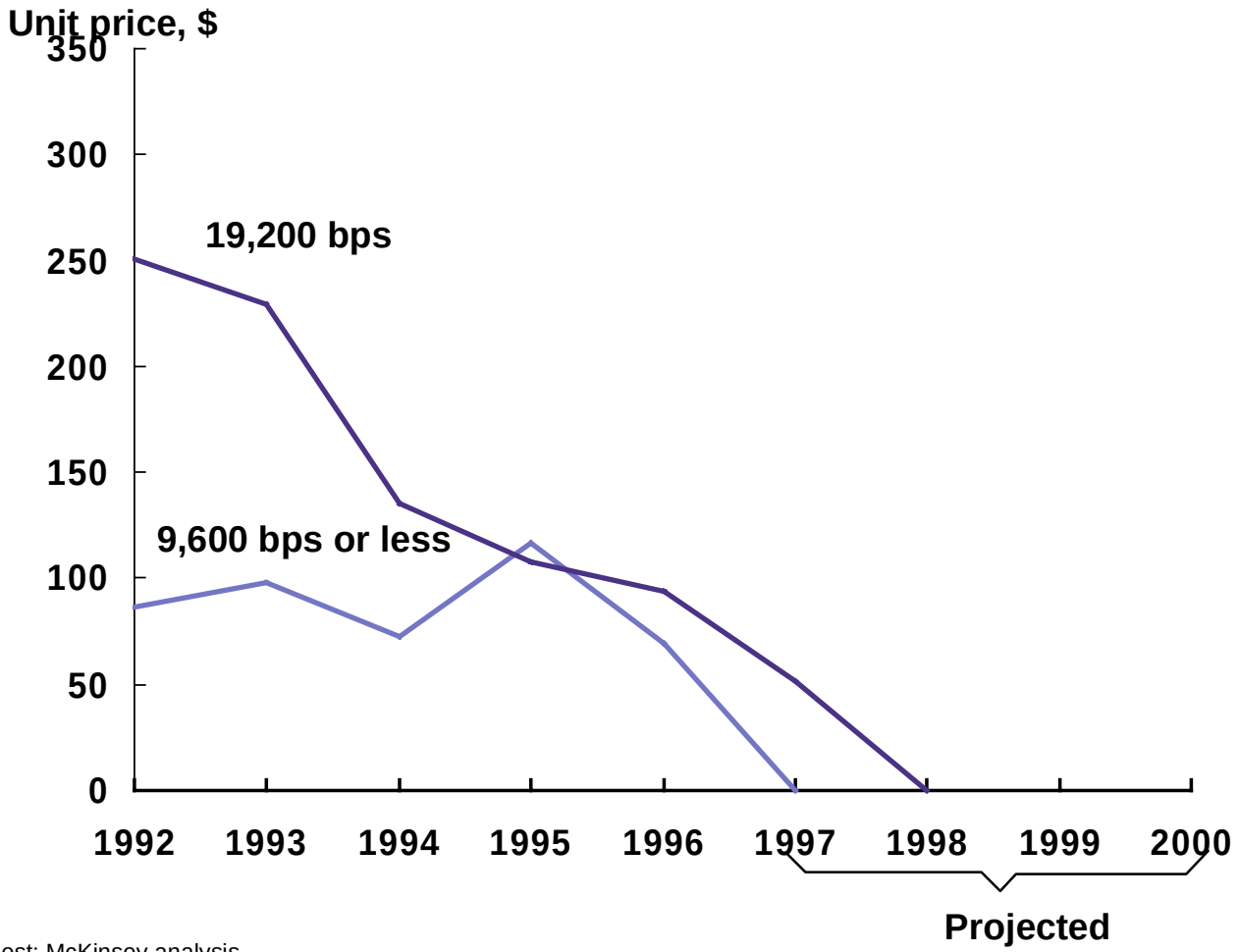
Modems shipped to North America



Source: Dataquest; McKinsey analysis

IMPACT OF SUBSTITUTION

Modems shipped to North America



Source: Dataquest; McKinsey analysis

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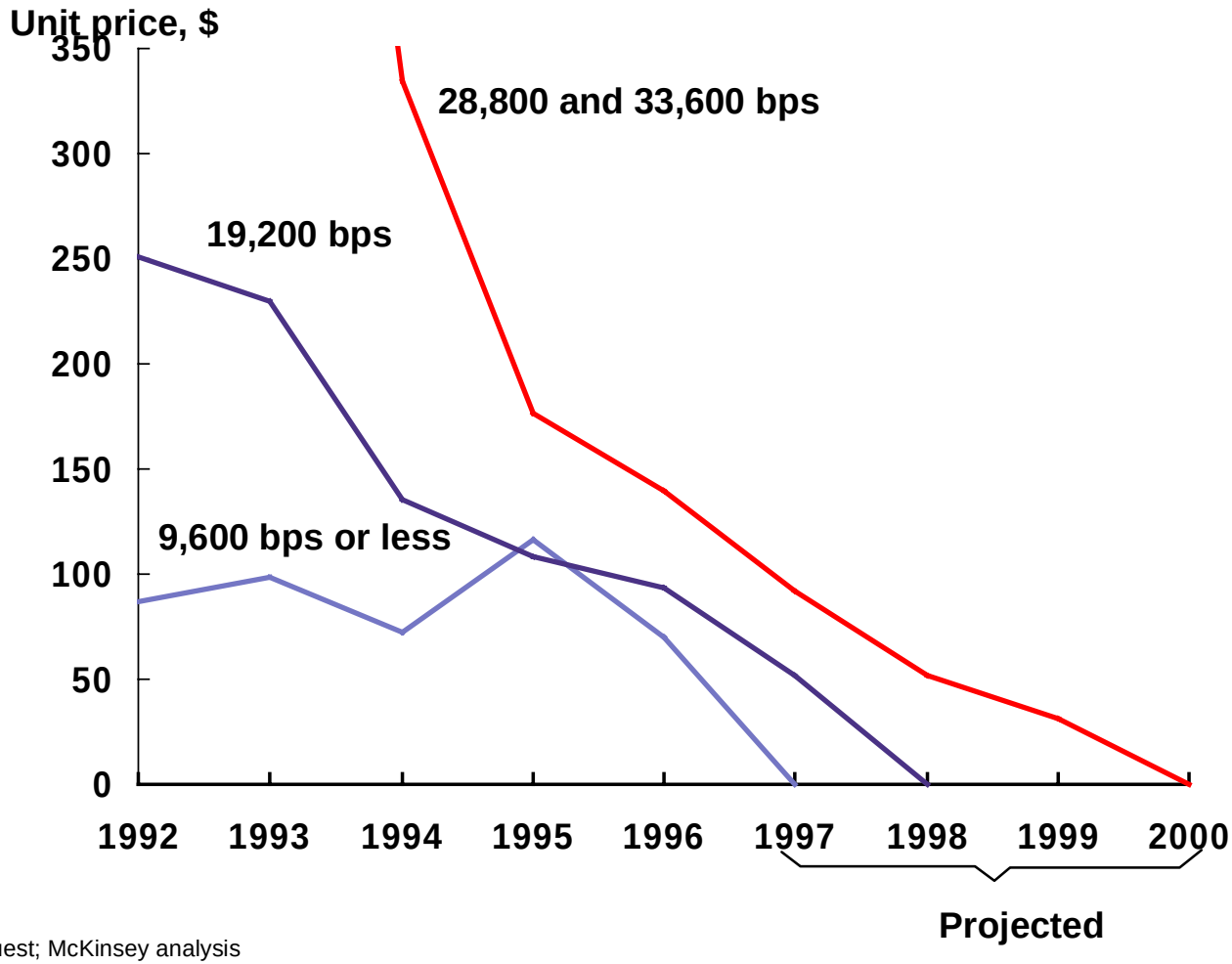
Modems shipped to North America



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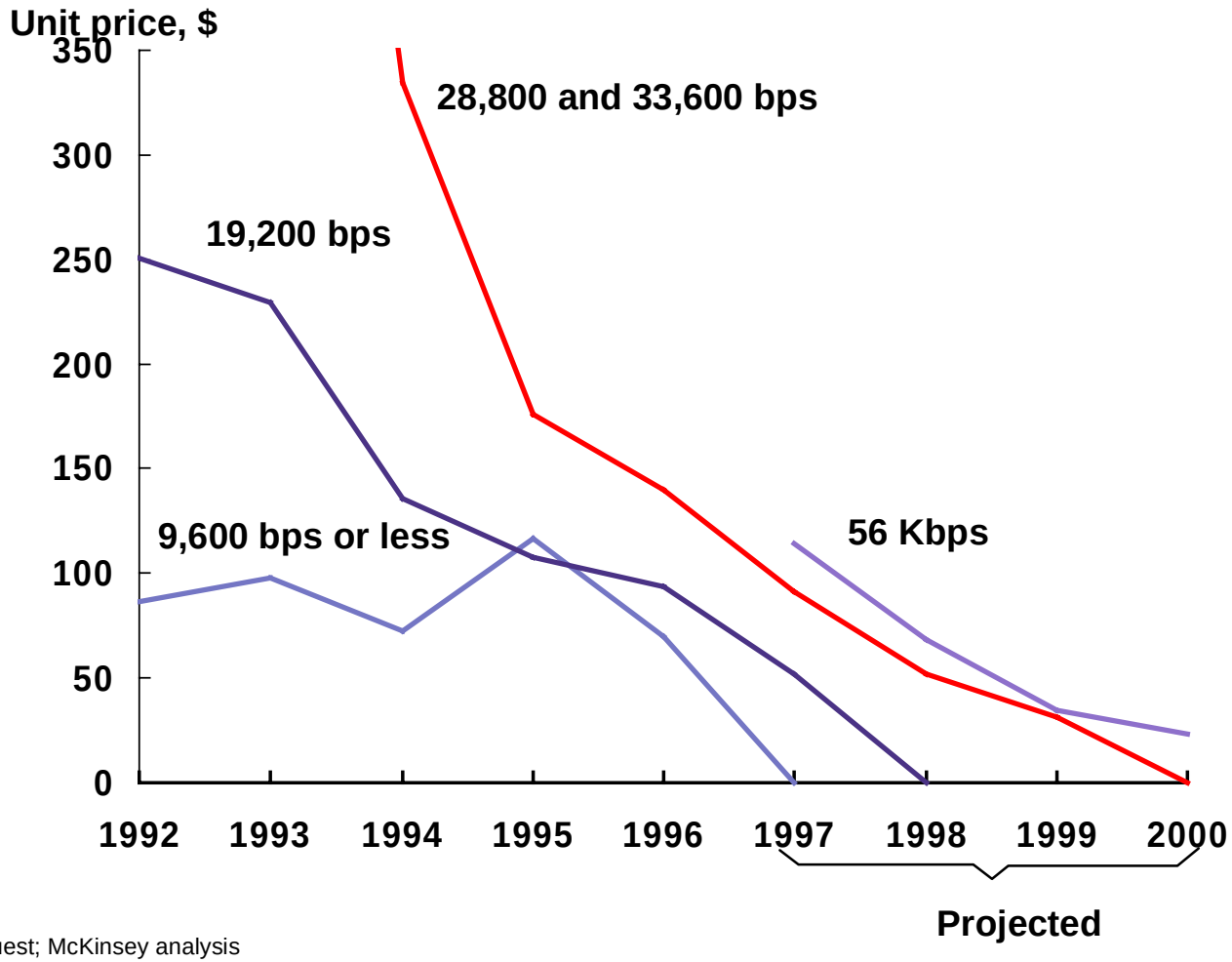
IMPACT OF SUBSTITUTION

Modems shipped to North America



Source: Dataquest; McKinsey analysis

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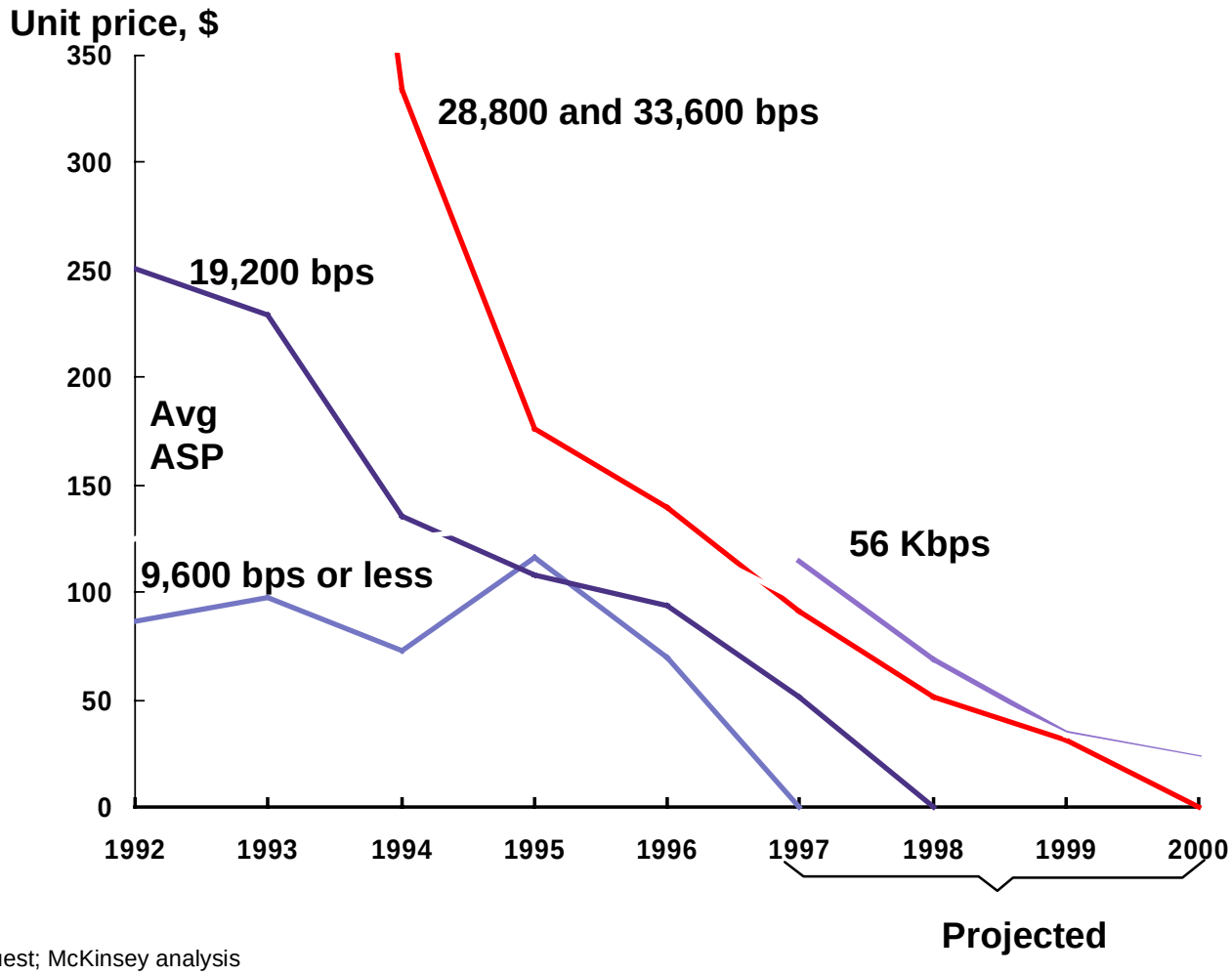
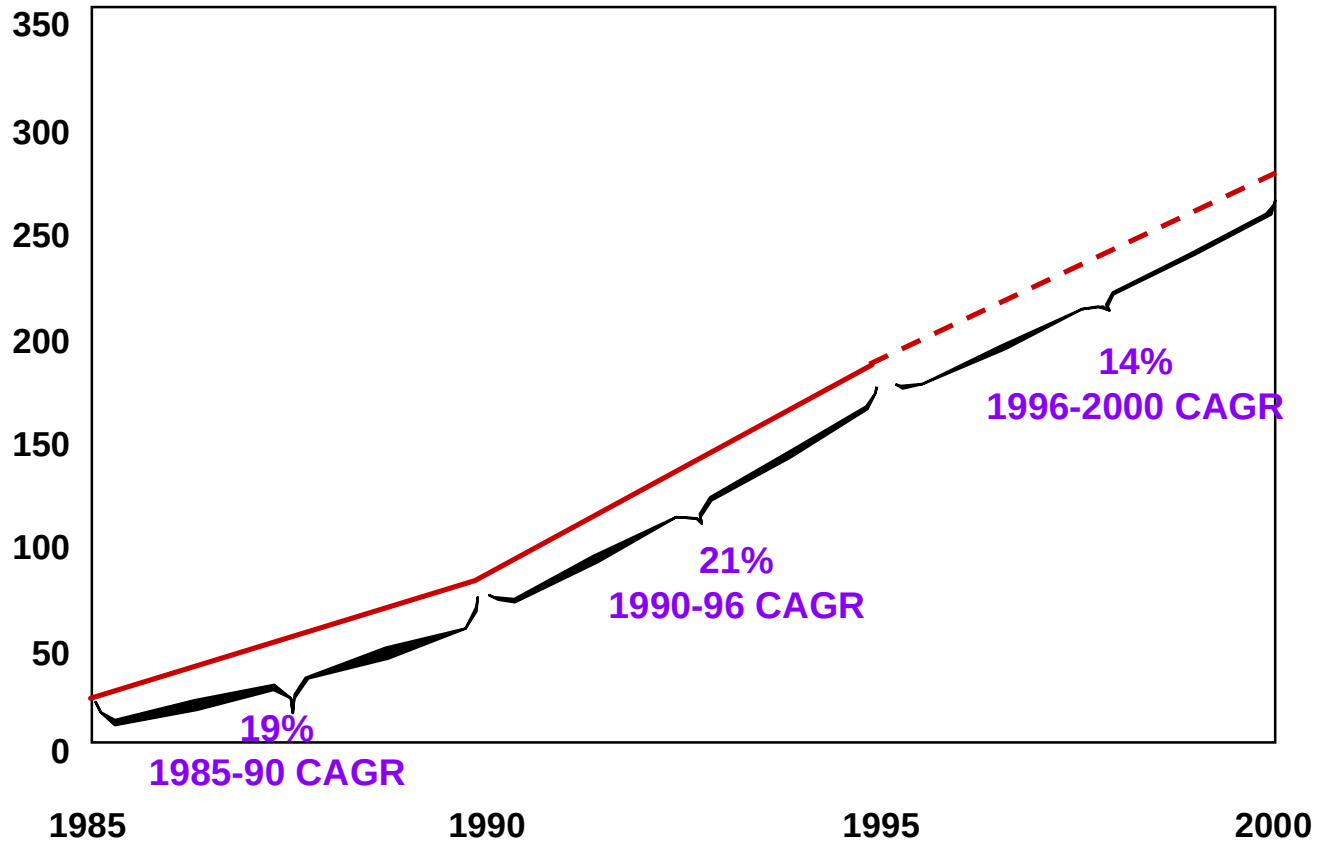


Source: Dataquest; McKinsey analysis

WORLDWIDE SEMICONDUCTOR REVENUES GROWING RAPIDLY

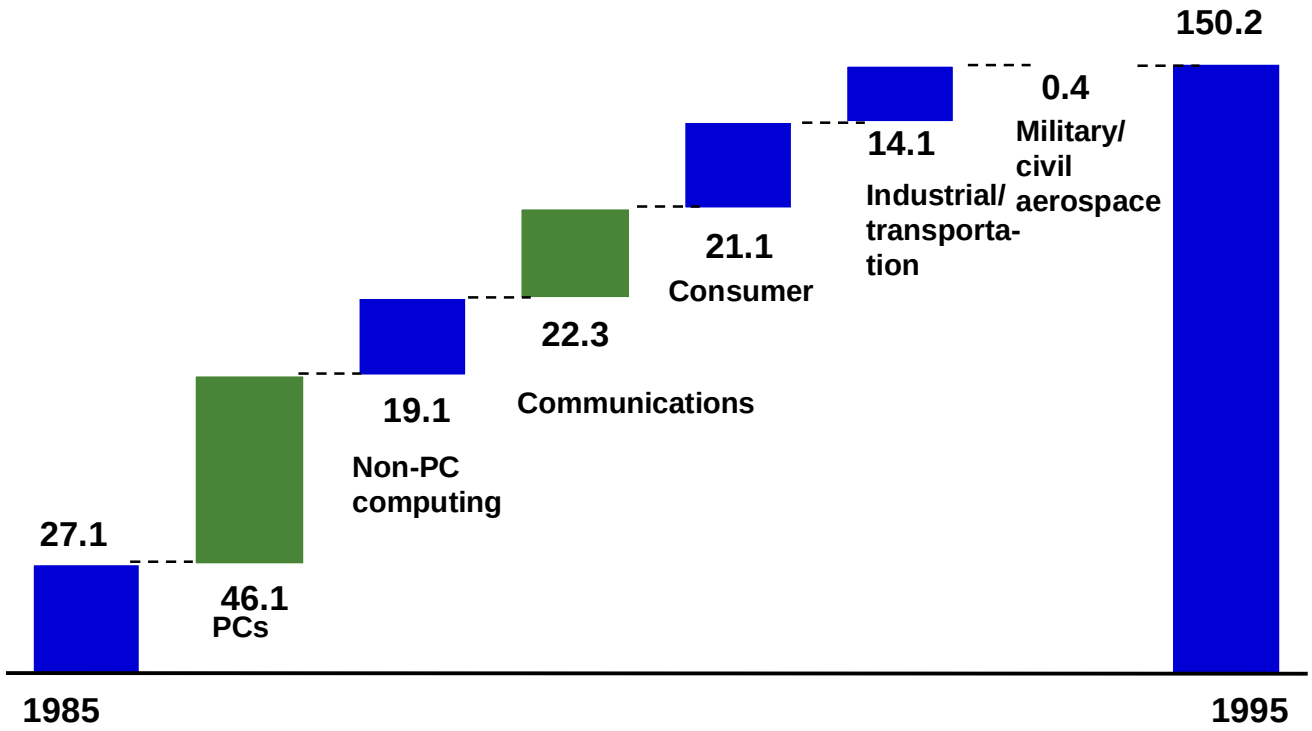
Merchant semiconductor sales, $ Billions



Source: ICE, Dataquest

PC INDUSTRY LARGE DRIVER OF GROWTH FROM 1985-1995

$ Billions

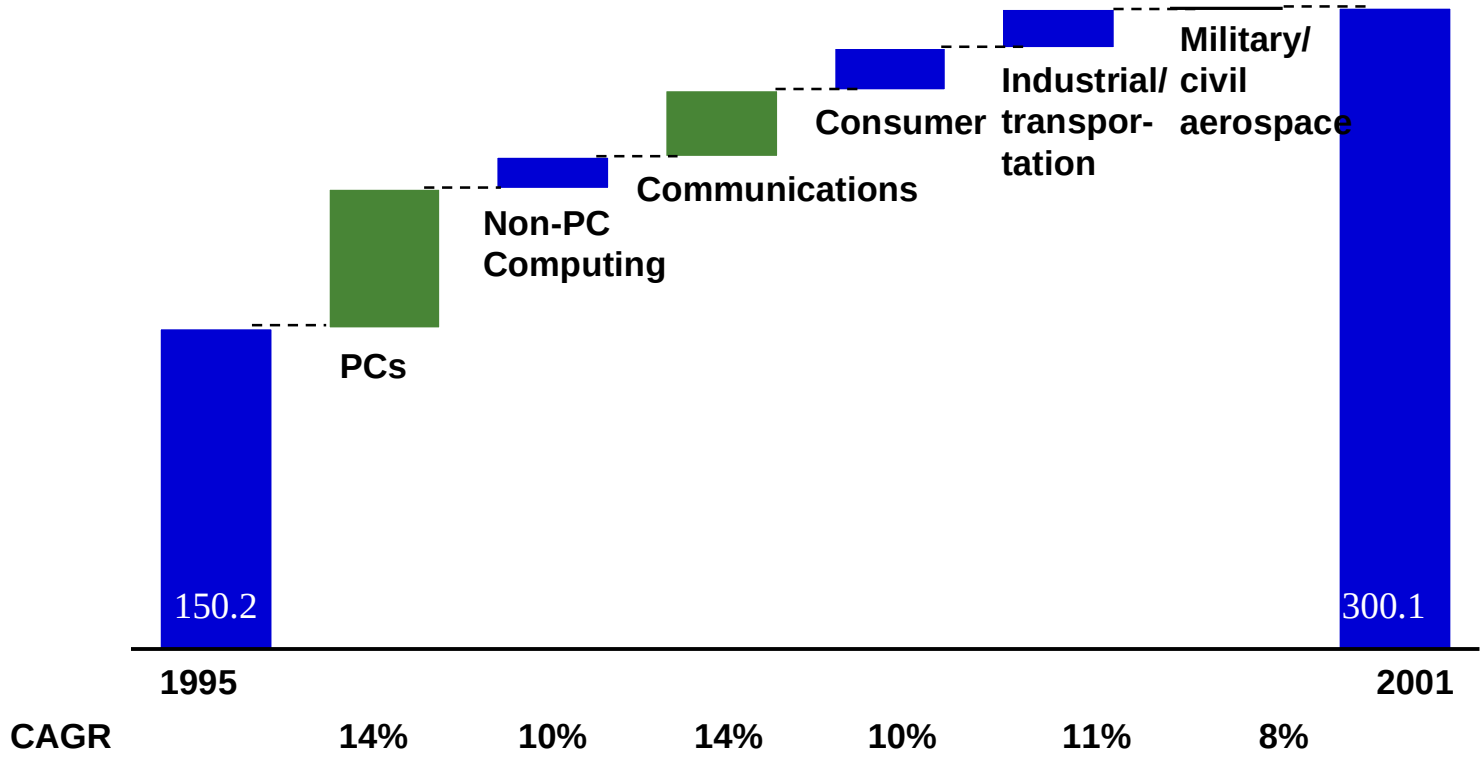


CAGR		34%	14%	21%	14%	14%	1%

Source: Dataquest; ICE status

PCs AND COMMUNICATIONS EXPECTED TO DRIVE GROWTH THROUGH 2001

$ Billions



Source: Dataquest (October 1997)

WINNERS HAVE PROFITED HANDSOMELY
Financial performance of leading players

Segment	Company	Average operating margins, 1992-96	Average ROIC, 1992-96
Memory (mostly DRAM)	Micron	23	34
Micro-processors	Intel	32	42
Program-mable logic ICs	Xilinx	27	42
Foundry	TSMC	32	25

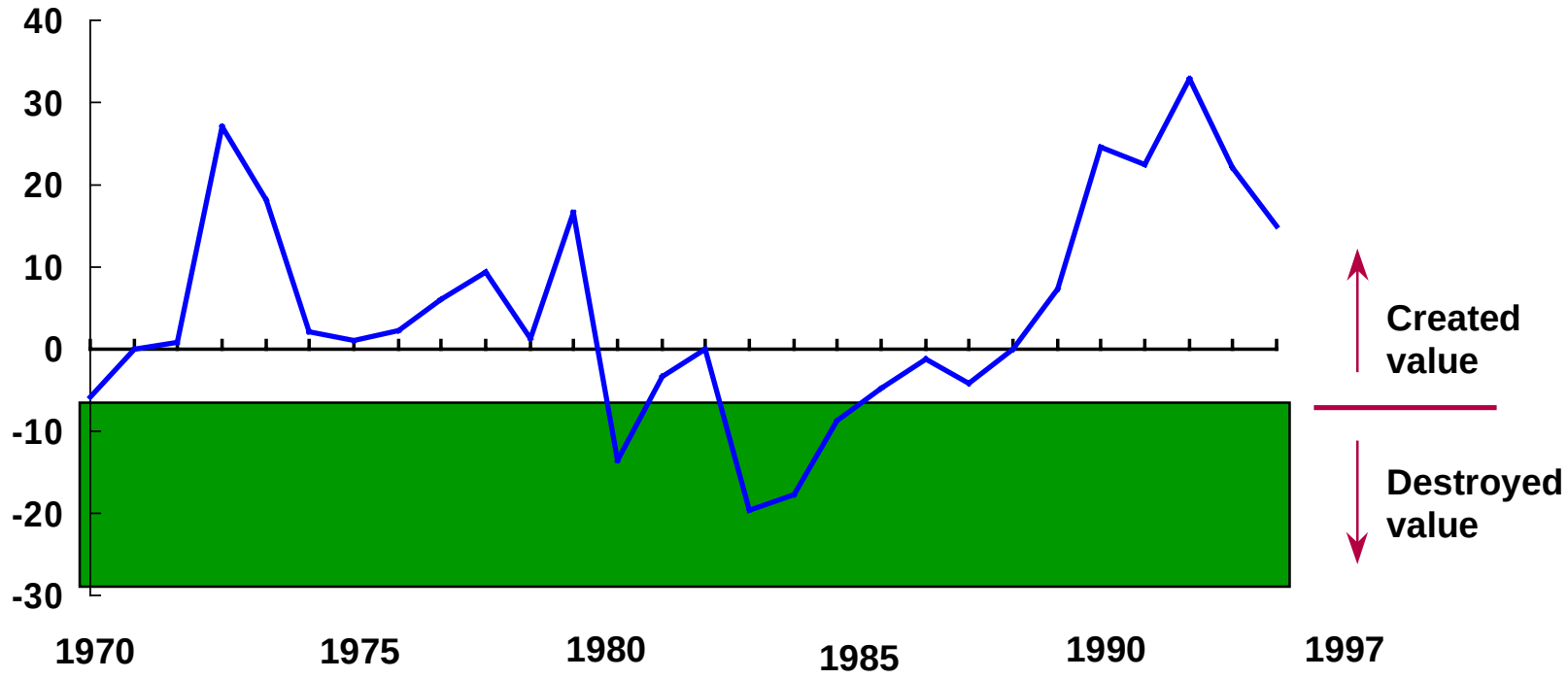
Percent

Source: 10Ks; McKinsey Corporate Finance Practice; Annual reports

UNATTRACTIVE INDUSTRY RESULTS

Economic profit margin of U.S. semiconductor companies

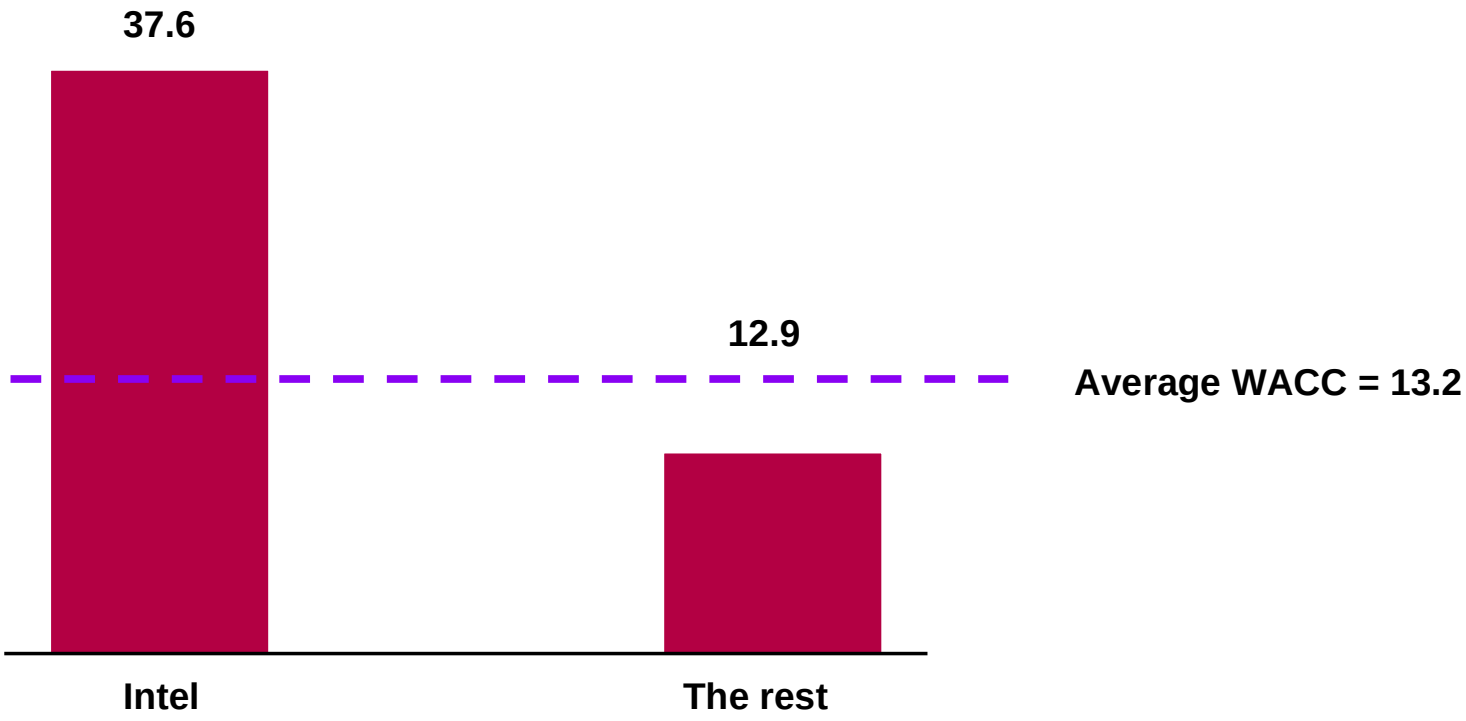
Percent



Note: Economic profit margin is weighted (ROIC-WACC) for AMD, Analog, Cypress, IDT, Intel, LSI Logic, Micron, National, VLSI (and TI from 1995)
Source: Annual reports; Compustat

INTEL'S PROFITABILITY HAS CARRIED THE INDUSTRY

Average ROIC, 1990-97



* Includes AMD, Analog Devices, Cypress, Cirrus Logic, LSI, Micron, National, VLSI, and TI

Source: Annual reports; Compustat

Background

The Seven Views of Computer Systems

Bell, Mudge & McNamara

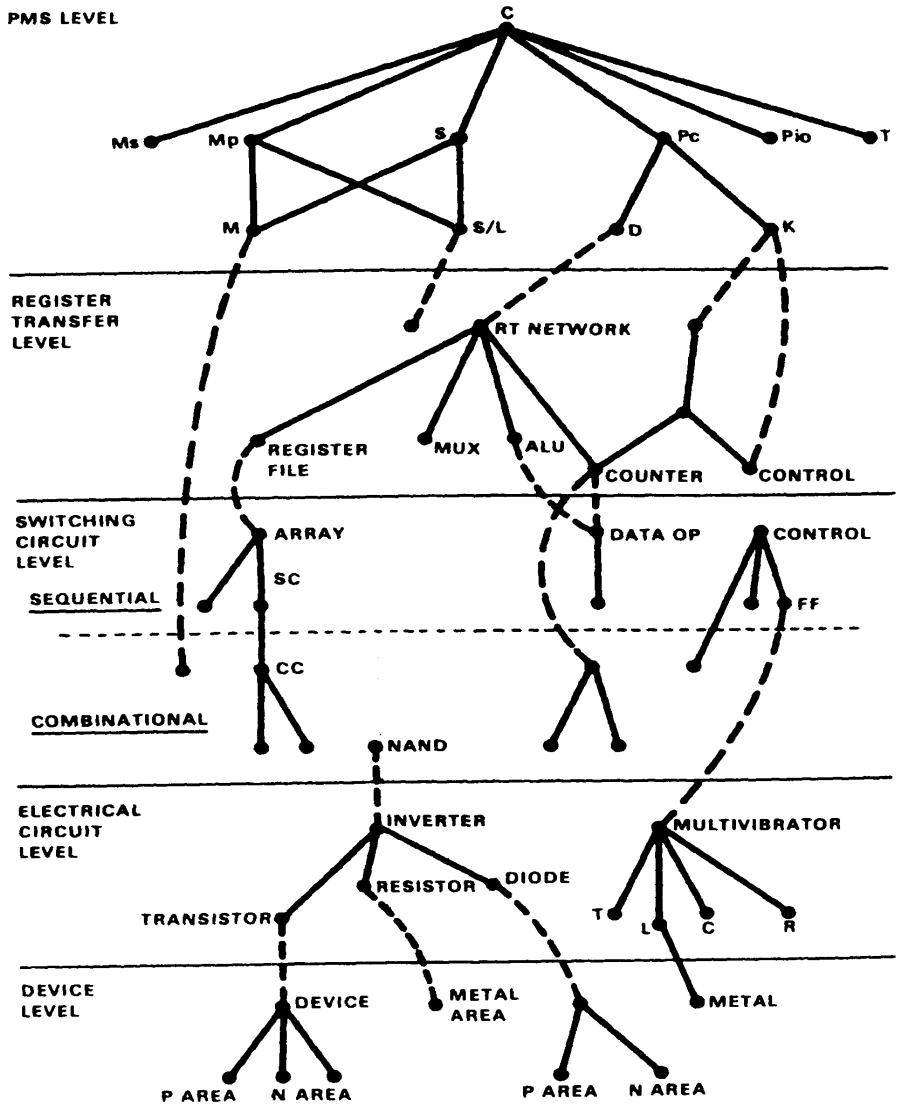
Source: Bill Lattin, Synopsys

The Seven Views of Computer Systems

View One:	Structural Levels of a Computer System
View Two:	Levy's Levels of Interpreters
View Three:	Packaging Levels of Integration
View Four:	A Marketplace View of Computer Classes
View Five:	An Applications/Functional View of Computer Classes
View Six:	The Practice of Design
View Seven:	The BLAAUW Characterization of Computer Design

Source: Bill Lattin, Synopsys

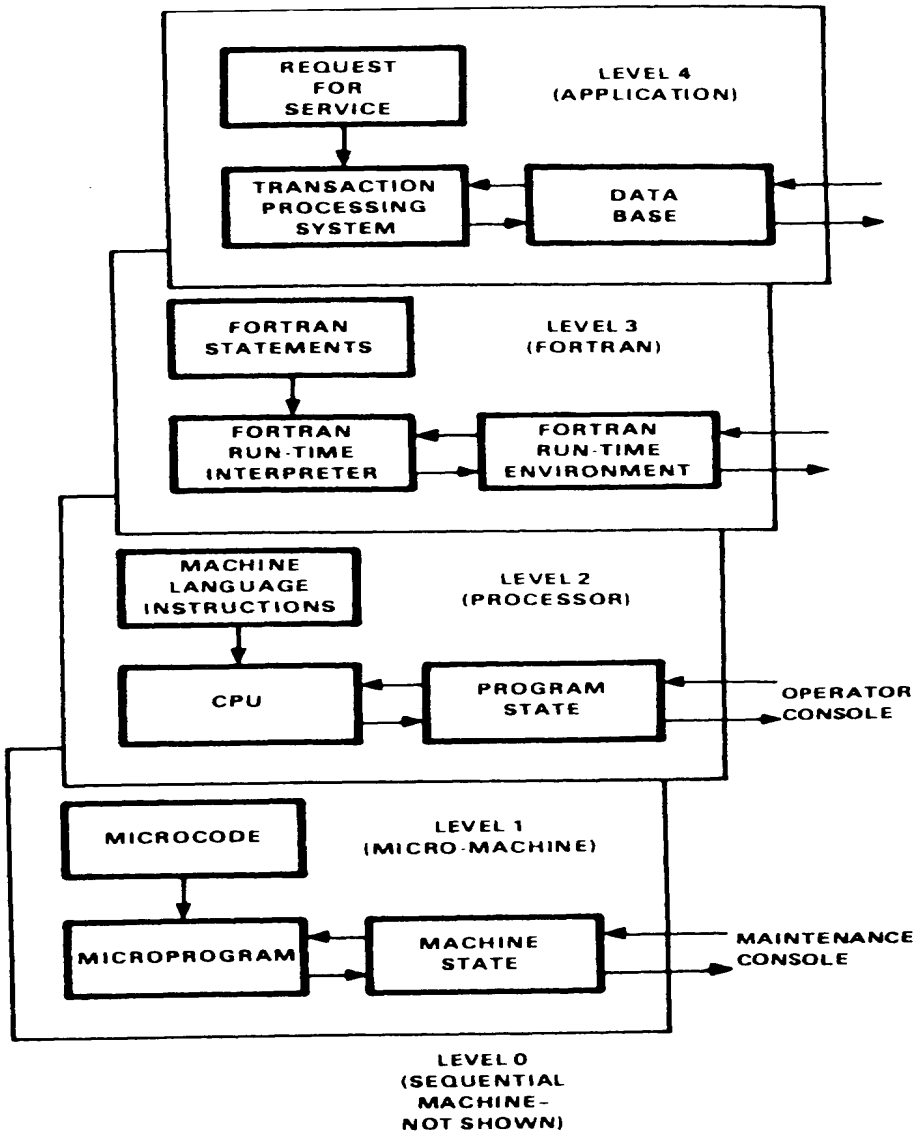
View One: Hierarchy of Computer Levels



Adapted from
Bell and Newell [1971]

Source: Bill Lattin, Synopsys

View Two: A Hierarchy of Interpreters



[Levy, 1974]

Source: Bill Lattin, Synopsys

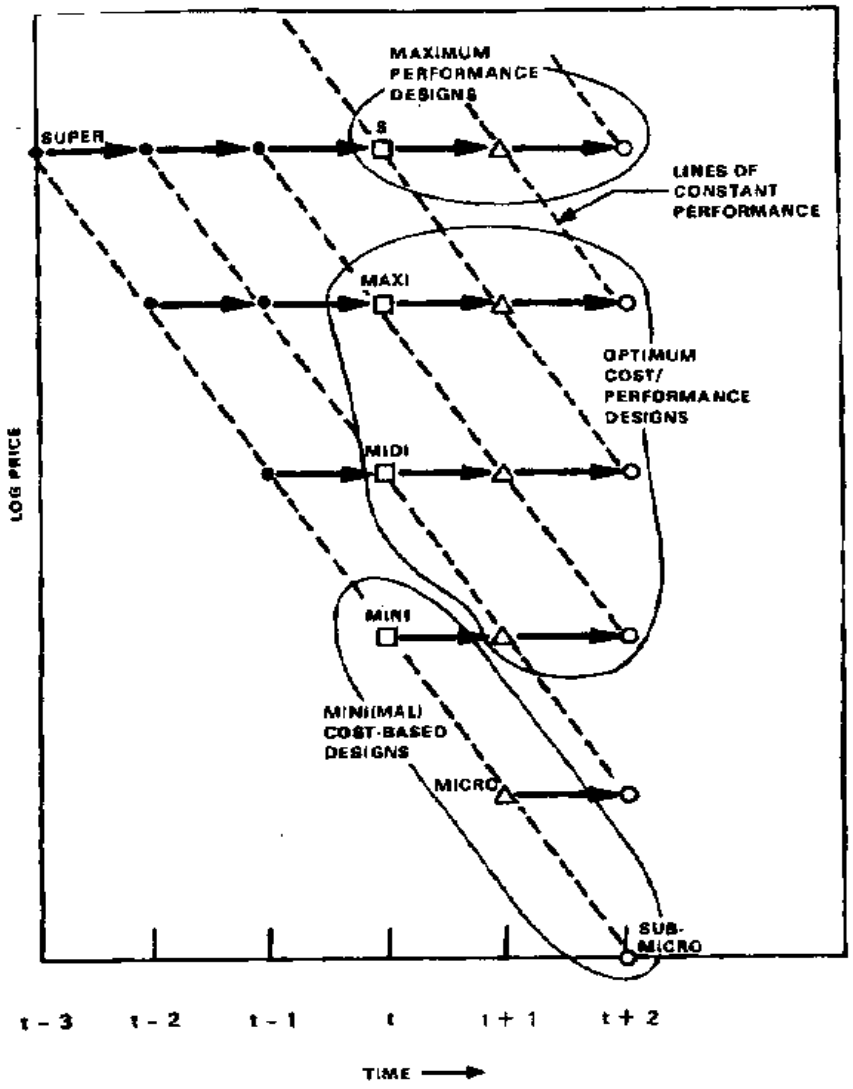
View Three: Packaging Levels of Integration

- This is a Structural View That Packages the Various Components (Hardware and Software) into Levels. The Levels for DEC Computers in 1978 Were as Follows:

→ **9**	Applications
→ **8**	Applications Components
→ **7**	Special Languages
→ **6**	Standard Languages
→ **5**	Operating Systems
→ **4**	Cabinets (to Hold Complete Hardware Systems)
→ **3**	Boxes
→ **2**	Modules (Printed Circuit Boards)
→ **1**	Integrated Circuits

Source: Bill Lattin, Synopsys

View Four: A Marketplace View of Computer Classes



Price vs. Time for Each Machine Class

Source: Bill Lattin, Synopsys

View Five: An Applications/ Functional View of Computer Classes

- ***PMS Level Configuration:*** A Configuration is Chosen to Match the Function to Be Performed. The User (Designer) Chooses the Amount of Primary Memory, the Number and Types of Secondary Memory, the Types of Switches, and the Number and Types of Transducers to Suit His Particular Application.

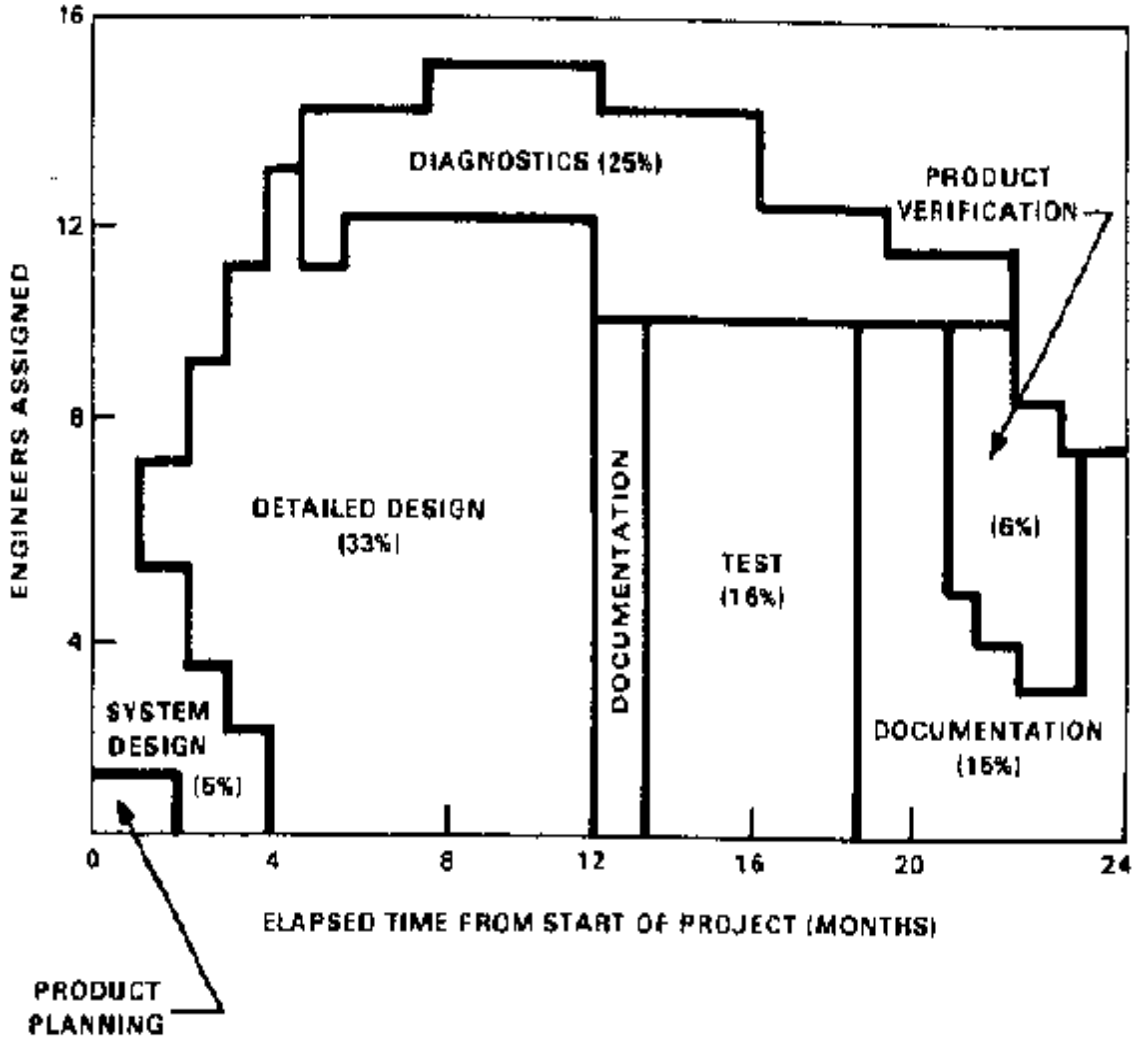
- ***Physical Packaging:*** Special Environmental Packaging is Used to Specialize a Computer System for Certain Environments, Such as Factory Floor, Submarine, or Aerospace Applications.

- ***Data-type Emphasis:*** Computers are Designed with Data-types (and Operations to Match) that are Appropriate to Their Tasks. Some Emphasize Floating-point Arithmetic, Others String Handling. Special-Purpose Processors, Such as Fast Fourier Transform Processors,Belong in This Category Also.

- ***Operating System:*** The Generality of the Computer is Used to Program Operating Systems That Emphasize Batch, Time Sharing,Real-Time, or Transacting Processing Needs.

Source: Bill Lattin, Synopsys

View Six: The Practice of Design



Hardware Development Costs for Developing a $50K Processor in '74

[Phister,1976]

Source: Bill Lattin, Synopsys

View Seven: The Blaauw Characterization of Computer Design

Characteristics of Design Areas

	Architecture	Implementation	Realization
Purpose	***Function***	***Cost and Performance***	***Buildable and Maintainable***
Product	Principles of operation	Logic design	Release to manufacturing
Language	Written algorithms	Block diagram, expressions	Lists and diagrams
Quality measure	Consistency	Broad scope	Reliability
Meanings (used herein)	ISP Machine ISP	RT level machine; microprogrammed sequential machine (at logic level)	Physical realization; physical implementation

Source: Bill Lattin, Synopsys

The Five Views of System on a Chip

View One: Semiconductor Process & Packaging View

View Two: IP Functional View

View Three: IP Design Methodology View

View Four: System Design Methodology View

View Five: System Software View

Source: Bill Lattin, Synopsys

View One: Semiconductor Process & Packaging View

- SIA Roadmap

→

THE CHALLENGES OF CHANGING CHIPS

Category	Problem	Key parameters	Trends					
tendency			**1995**	**1998**	**2001**	**2004**	**2007**	**2010**
Complexity increase	Will challenge fault isolation	Number of logic transistors, in millions	12	14	26	50	210	430
		I/O	900	1350	2000	2600	3600	4800
		Wiring levels	4-5	5	5-6	6	6-7	7-8
		Chip size	250 mm^2	300 mm^2	360 mm^2	430 mm^2	520 mm^2	620 mm^2
Dimension	Will require	Minimum feature size	0.35 μm	0.25 μm	0.18 μm	0.13 μm	0.1 μm	0.07 μm
decrease	higher-powered,	Minimum defect size	0.12 μm	0.08 μm	0.06 μm	0.04 μm	0.03 μm	0.02 μm
	slower inspection	Interlevel contact diameter	0.4 μm	0.28 μm	0.2 μm	0.14 μm	0.11 μm	0.08 μm
		Gate dielectric thickness	7-12 nm	4-5 nm	4-5 nm	4-5 nm	<4 nm	<4 nm
Performance	Will raise sensitivity	Logic clock speed	350 MHz	450 MHz	600 MHz	800 MHz	1000 MHz	1100 MHz
acceleration	to subtle, hard-to find facts	Threshold voltage variation	70 mV	50 mV	40 mV	30 mV	25 mV	20 mV
		Supply voltage	2.5-3.3 V	1.2-2.5 V	1.2-1.8 V	1.2-1.5 V	<1.2 V[a]	<1.2 V[a]
New materials	Will need new delayering techniques	Metal wiring		Al			Al, Cu	
		Insulator	Oxide		Oxide, air, polyimide, low dielectric			
New styles of packaging	Will force physical fault isolation to be done from back of chip	Flip-chip, chip-on-board (COB), chip-on-chip	–	–	–	–	–	–

Data from National Technology Roadmap for Semiconductors, 1994, Semiconductor Industry Association

Source: Bill Lattin, Synopsys

Conclusions From View One

- 20M Gates will be Here in 2000
- Multiple Power Supplies will Require DCL Descriptions (Equations vs Tables)
- Copper is Here Now (6 Layers)
- Trench DRAM Hybrid Process in 1999
- I/O Continue to Grow (Power Management EMI Analysis & Synthesis)

Source: Bill Lattin, Synopsys

View Two: IP Functional View

- ***Microprocessor***
- ***Memory Sub System***
- ***ASIC (Customer's Logic)***
- ***DSP***
- ***RF (Analog)***
- ***Mixed Signal***
- ***I/O Systems***
- ***On Chip Bus***

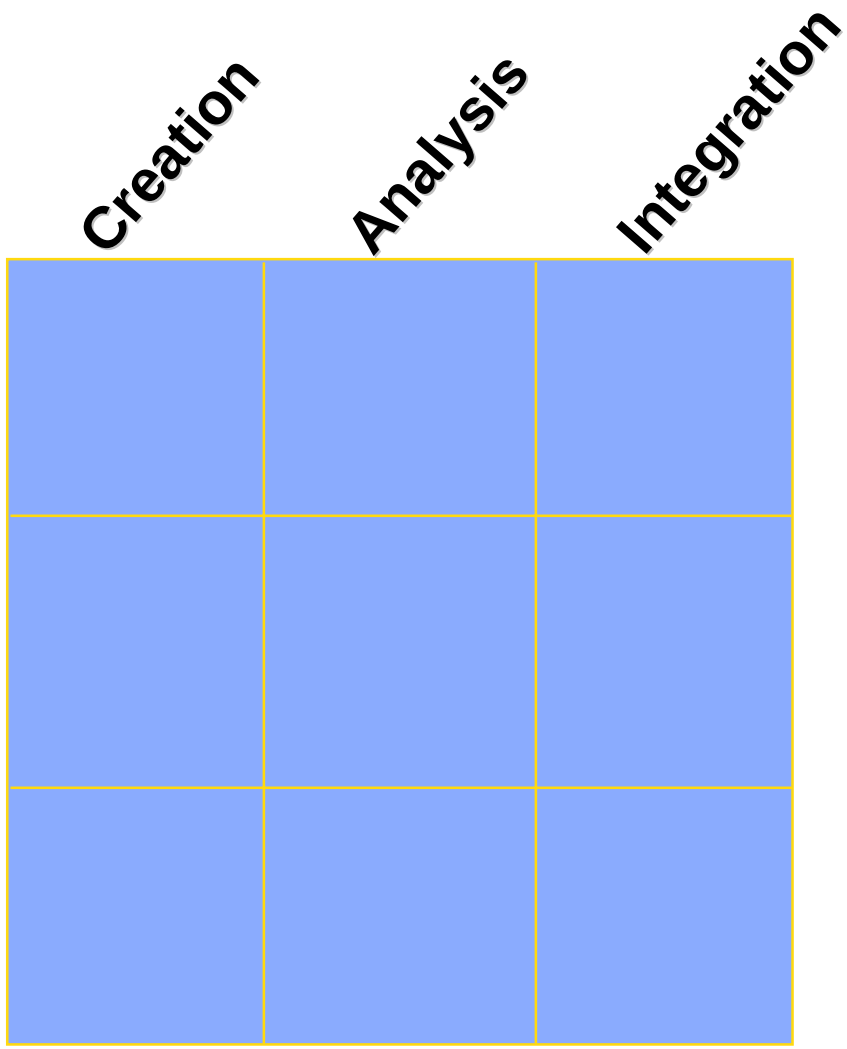
Source: Bill Lattin, Synopsys

View Three: IP Design Methodology

Creation

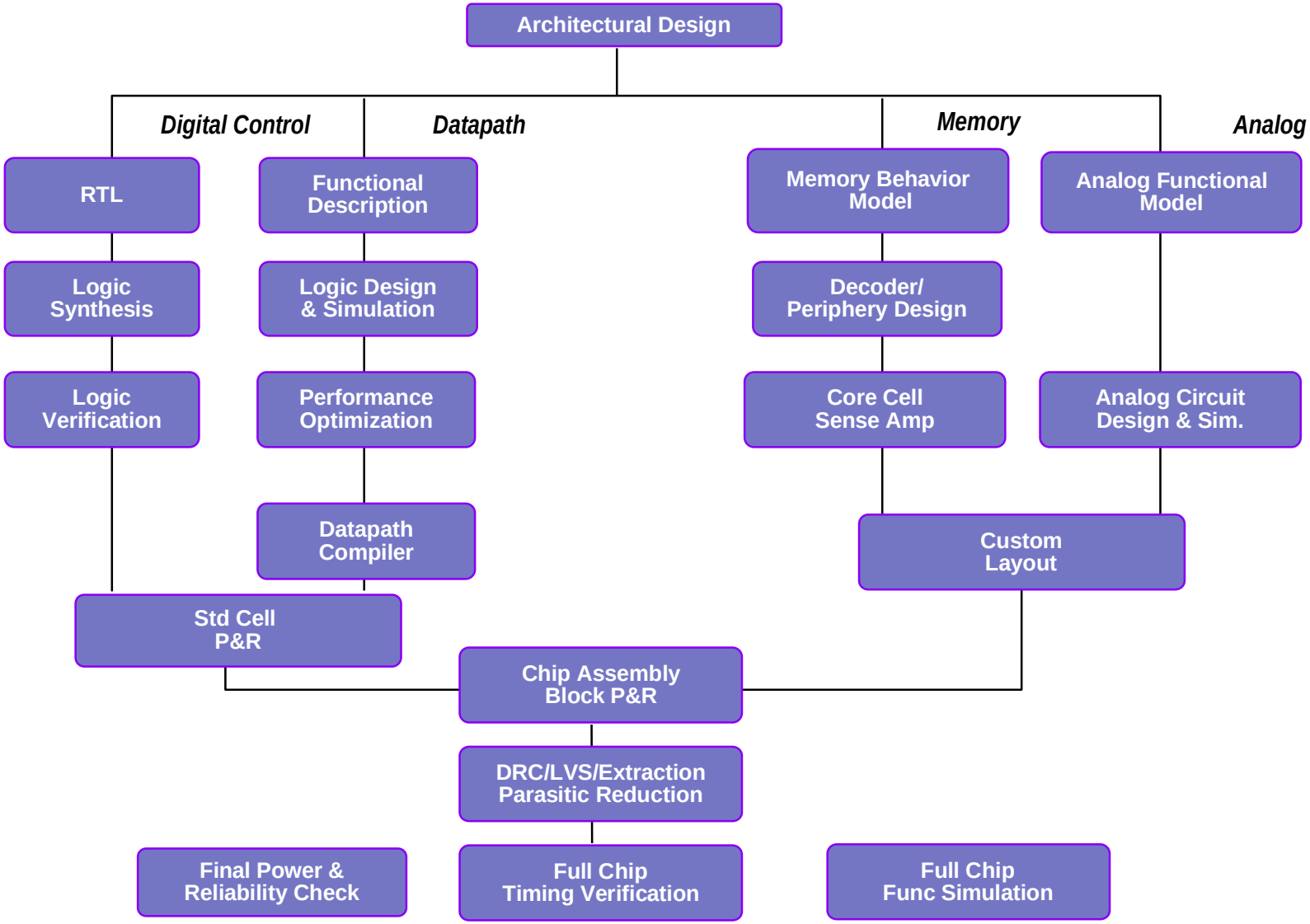
Analysis

Integration



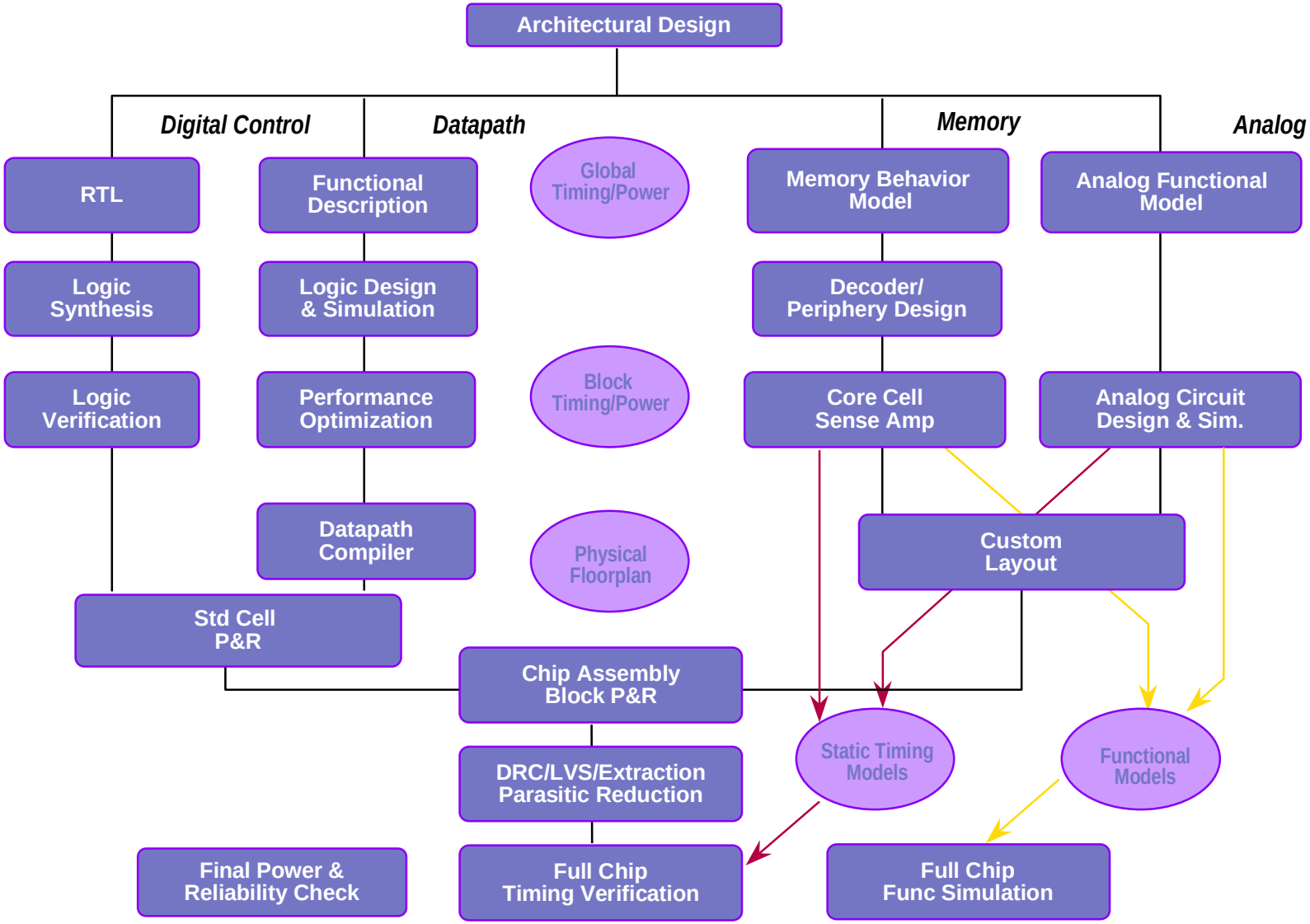
Source: Bill Lattin, Synopsys

System-on-a-Chip IP Creation and Analysis Flow



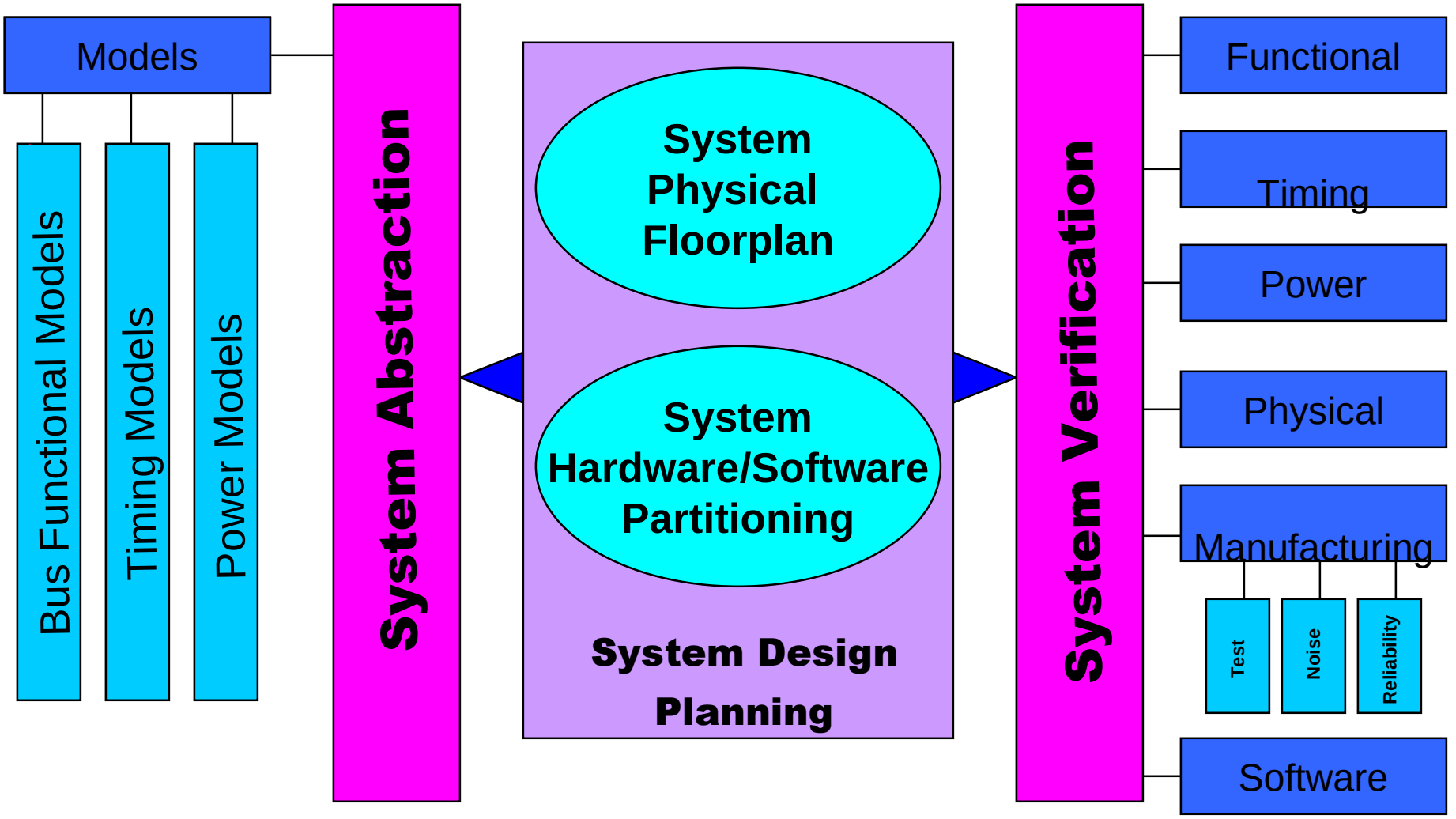
Source: Bill Lattin, Synopsys

System-on-a-Chip Design Flow



Source: Bill Lattin, Synopsys

System-on-a-Chip Integration Flow



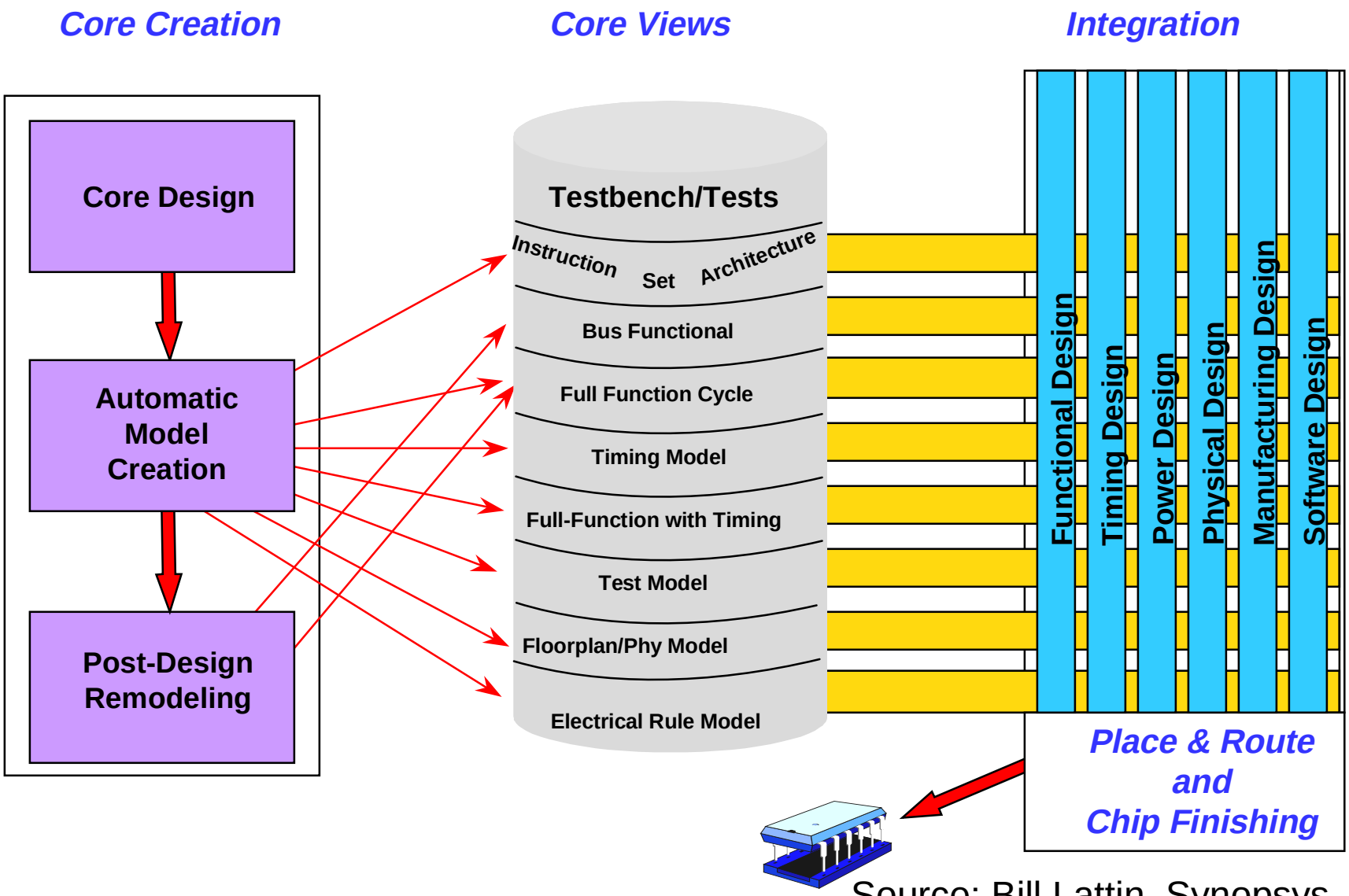
Source: Bill Lattin, Synopsys

View Four - System Design Methodology

- Problems Migrate to the IP Block Boundaries
- IP Blocks Effect Each Other
- Tools Must Enforce IP Block Boundaries
- IP Blocks Need Different Analysis Tools
  - ✔Digital IP Blocks
  - ✔Mixed Signal IP Blocks
  - ✔RF IP Blocks
  - ✔Memory IP Blocks

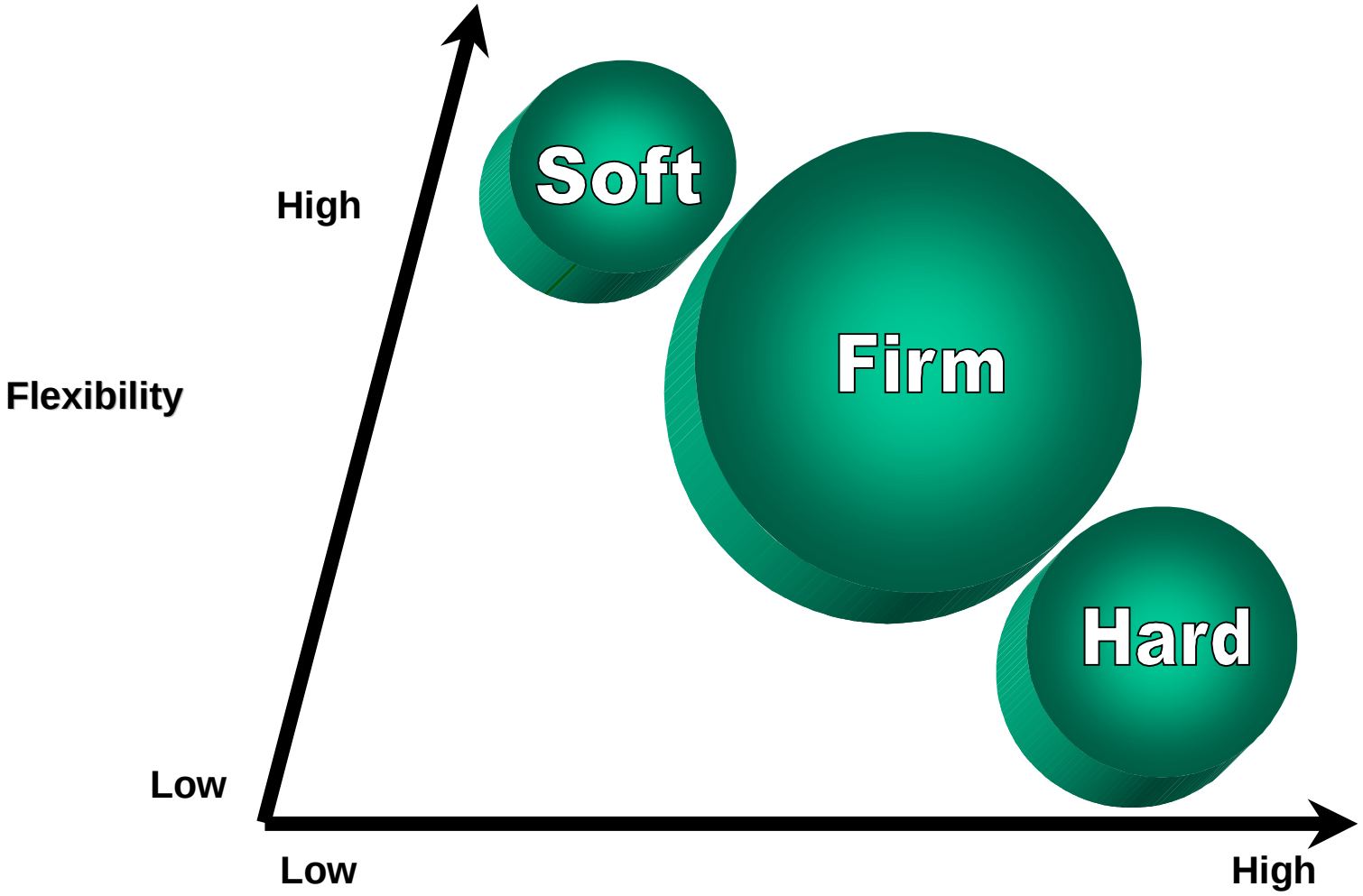
Source: Bill Lattin, Synopsys

SoC Model Views



Source: Bill Lattin, Synopsys

Tradeoffs Among Types of System Designs



Predictability, performance, and complexity

Source: Bill Lattin, Synopsys