Summary of Viterbi Estimates

Philip Chong	StrongARM Implementation
Rhett Davis, Ning Zhang David Chinnery	ASIC
Niraj Shah, Scott Weber	Configurable Microprocessor
Paul Husted	TMS320VC5402 DSP

ASIC

- 0.25um technology, 1.0V supply
- estimates for power, area and speed based on ACS unit, survivor memory unit and SRAM
- fully parallel structure with 64 states and 64 ACS cells all operating in parallel
- 3 blocks of 128 words of 64 bits SRAM (rounded to 3Kbytes)
- critical path is through the ACS unit

Implementation	Speed (kbps)	Power (mW)	Area (mm^2)	Design Time (work days)	Signal to Noise Degradation (dB)
ASIC	100	0.004	2.5	180	0.05

Configurable Microprocessor

- 32 bit RISC Tensilica microprocessor soft core
- 0.25um technology, 2.5V supply
- 16Kbyte cache

Implementation	Speed (kbps)	Power (mW)	Area (mm^2)	Design Time (work days)	Signal to Noise Degradation (dB)
Configurable Microprocessor	750	191.000	3.1	12	0.05

DSP

- TI TSMC320C54xx low power DSP chip highly optimized to perform Viterbi decoding
- ALU with single compare, select and store unit to compare branch metrics and record the larger value storing the decision bit
- 40Kbyte cache

Implementation	Speed (kbps)	Power (mW)	Area (mm^2)	Design Time (work days)	Signal to Noise Degradation (dB)
DSP	582	158.000	144.0	5	0.05

StrongARM

- StrongARM SA-1100, 0.35um technology
- has barrel shifter allowing variable length bit shifts in single cycle
- 32 bit fixed point arithmetic (presumably under 0.05dB degradation)
- table lookup to determine code bits for each branch hypothesis
- may increase bit rate by 10% by loop unrolling

Implementation	Speed (kbps)	Power (mW)	Area (mm^2)	Design Time (work days)	Signal to Noise Degradation (dB)
StrongARM	100	550.000	60.0	several	0.00
scaled to 0.25um	100	400.000	30.0	several	0.00

Summary

Implementation	Speed (kbps)	Power (mW)	Area (mm^2)	Design Time (work days)	Signal to Noise Degradation (dB)
ASIC	100	0.004	2.5	180	0.05
Configurable Microprocessor	750	191.000	3.1	12	0.05
DSP	582	158.000	144.0	5	0.05
StrongARM	100	400.000	30.0	several	0.00

Normalized to 100kbps:

Implementation	Speed (kbps)	Power (mW)	Area (mm^2)	Design Time (work days)	Signal to Noise Degradation (dB)
ASIC	100	0.004	2.5	180	0.05
Configurable Microprocessor	100	25.000	3.1	12	0.05
DSP	100	27.000	144.0	5	0.05
StrongARM	100	400.000	30.0	several	0.00

Power-Area Products

Normalized to 100kbps:

Implementation	Power (mW)	Area (mm^2)	Power x Area (mW mm^2)	Design Time (work days)	Signal to Noise Degradation (dB)
ASIC	0.004	2.5	0.01	180	0.05
Configurable Microprocessor	25.000	3.1	78.00	12	0.05
DSP	27.000	144.0	3900.00	5	0.05
StrongARM	400.000	30.0	12000.00	several	0.00

Normalized power-area product:

Implementation	Power (mW)	Area (mm^2)	Normalised Power x Area	Design Time (work days)	Signal to Noise Degradation (dB)
ASIC	0.004	2.5	1	180	0.05
Configurable Microprocessor	25.000	3.1	7800	12	0.05
DSP	27.000	144.0	390000	5	0.05
StrongARM	400.000	30.0	1200000	several	0.00