EECS 244: Introduction to CAD and the Course

Prof. Kurt Keutzer

EECS

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Lecture Overview

- Introduction to Kurt, Sanjit, …. and others
- Education and your future career
- CAD, Semiconductors and the broader economy
- Brief overview of CAD
- Goals of course

Skills you Will Need

- Wherever you go, after you graduate you will find yourself in a complex environment requiring knowledge and mastery over a variety of fields
  - In the good old days:
    - Ph. D's join a university (e.g. Berkeley) or company (e.g. IBM) for life
    - Work locally in a single geographic area within an ethnically homogeneous group for entire career
    - Business concerns handled by "management"
    - Engineers left to focus on purely technical problems
    - Technical problems narrowly focused - coding theory, queuing theory, analog circuit design etc.
  - New era
    - Moving around companies, universities, and geographies is the norm
    - Professors and engineers must create a "business case" for their research which lays out a plan for impact on business (i.e. revenue) or defense
    - Professor or engineer you need to be a complete corporation of size one with marketing and sales as well as engineering
    - Technical problems complex and interdisciplinary. A system-on-a-chip is precisely that. A complex mix of HW, SW, user interface supporting a variety of applications

I hope you come to view this as an exciting opportunity. Your careers can be incomparably more interesting and satisfying than those of prior generations.

How do we get these skills?

- Educational process evolves relatively slowly
- EECS curriculum still principally focused on science and engineering
- Fortunately, the campus is diverse
- Specifically:
  - Engineering:
    - EECS curriculum focused on this and does a good to great job
  - Marketing
    - Strategic: Need to understand the broader economy, the *value chain,* and the key trends
    - Tactical: Need to understand customer needs and how to meet them
    - Need to understand how to merge these two – identify the right customer and meet their needs
    - Berkeley Management of Technology (MOT) program good at this
  - Sales
    - Need to *communicate* value to the end customer
    - Need to learn how to "close" the customer to get your ideas funded
    - Not sure how you're going to learn this but excellent communication skills is a good start
- Today we're going to a mini-course on marketing and CAD – warning – it may be the oddest first lecture you've ever had!!

Introduction to Kurt

- Professor in EECS
- B. S. in mathematics from Maharishi International University 1978 (yes, I'm serious)
- M. S., Ph.D. in CS from Indiana University 1984
- AT&T Bell Labs, Area 11 1984-1991
  - Developed a number of successful (internally) tools for hardware developers
    - Plaid – Programmable Logic AID – used to create racks of switching system hardware
    - DAGON – worked with Chuck Stroud and Mark Vancura to create a logic synthesis system for Bell Labs – dozens of IC's developed with the system

Introduction to Kurt

- Synopsys, Inc. 1991-1998 (now 14th largest software company)
  - From Member of Research Staff of $30M 200 person company to SVP/CTO of $600M 3000 person company in 7 years
  - As CTO
  - oversaw and reviewed technology of over 25 software products accounting for $600M in revenue
  - Identified new technology and market opportunities
  - Initiated and participated in a dozen corporate acquisitions
  - As Manager=>Director=>VP=>SVP or research
    - Initiated a number of product ideas and two complete products:
    - FPGA Express – FPGA synthesis software – brought to ``product roll-out''
    - Formality – market leader in formal verification of circuits –

UC Berkeley 1998-present

- Professor of EECS
  - As teacher – EECS 244 (Intro to CAD), CS169 (Software Engineering)
  - Associate Director – Gigascale Systems Research Center 1998-2001
  - As a research advisor
    - MESCAL: modern embedded systems, compilers, architectures, and languages – 8 students

Introduction to Kurt

As an entrepreneur:

- **Cadabra (acquired by Numerical Technology 2000, acquired by Synopsys 2003) – investor/Corporate Board**
- **Everest Design (acquired SNPS, 1999) – investor/TAB**
- **Right Track CAD (acquired by Altera, 2000) – angel investor/TAB**
- **0-in Design Automation – Series A investor 1998/TAB - acquired by Mentor Graphics 8/2004**
- **Tensilica, Inc (upside top 100), Series A investor 1998/TAB**
- **Catalytic Compilers – angel investor/TAB – founded Fall 2002, $6M in funding from NEA and ITU July 2003**
- **Stretch Inc. - Series A investor/TAB – founded 2002, $15M in funding from Worldview, July 2003**
- **CommandCad – Angel investor – founded 2004 –DFM start-up founded by Berkeley grad students**

- **As a consultant: Cadence (2001-present) Synopsys (1998 – 2000) Ammocore, C-Cube Microsystems (IPO), CoWare, Hier Design (acquired by Xilinx) Reshape, a number of venture capital firms**

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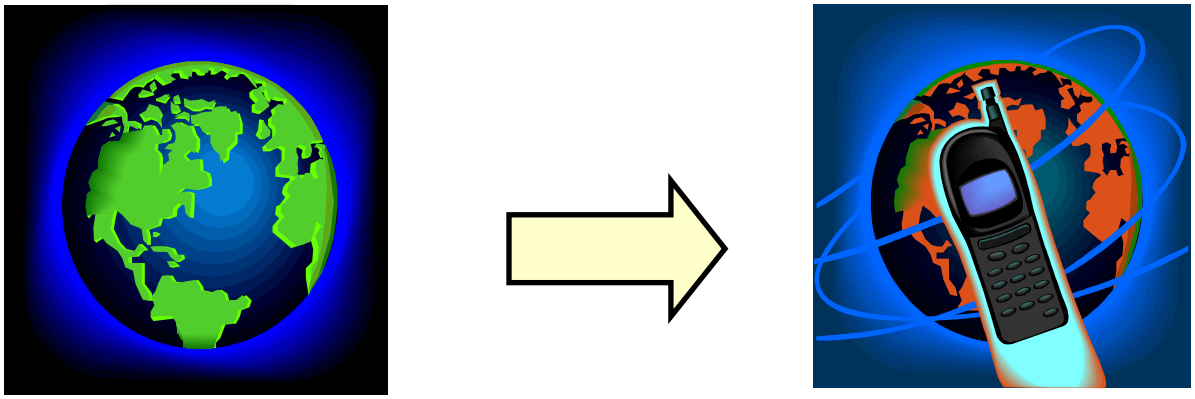
The World and Electronic Systems

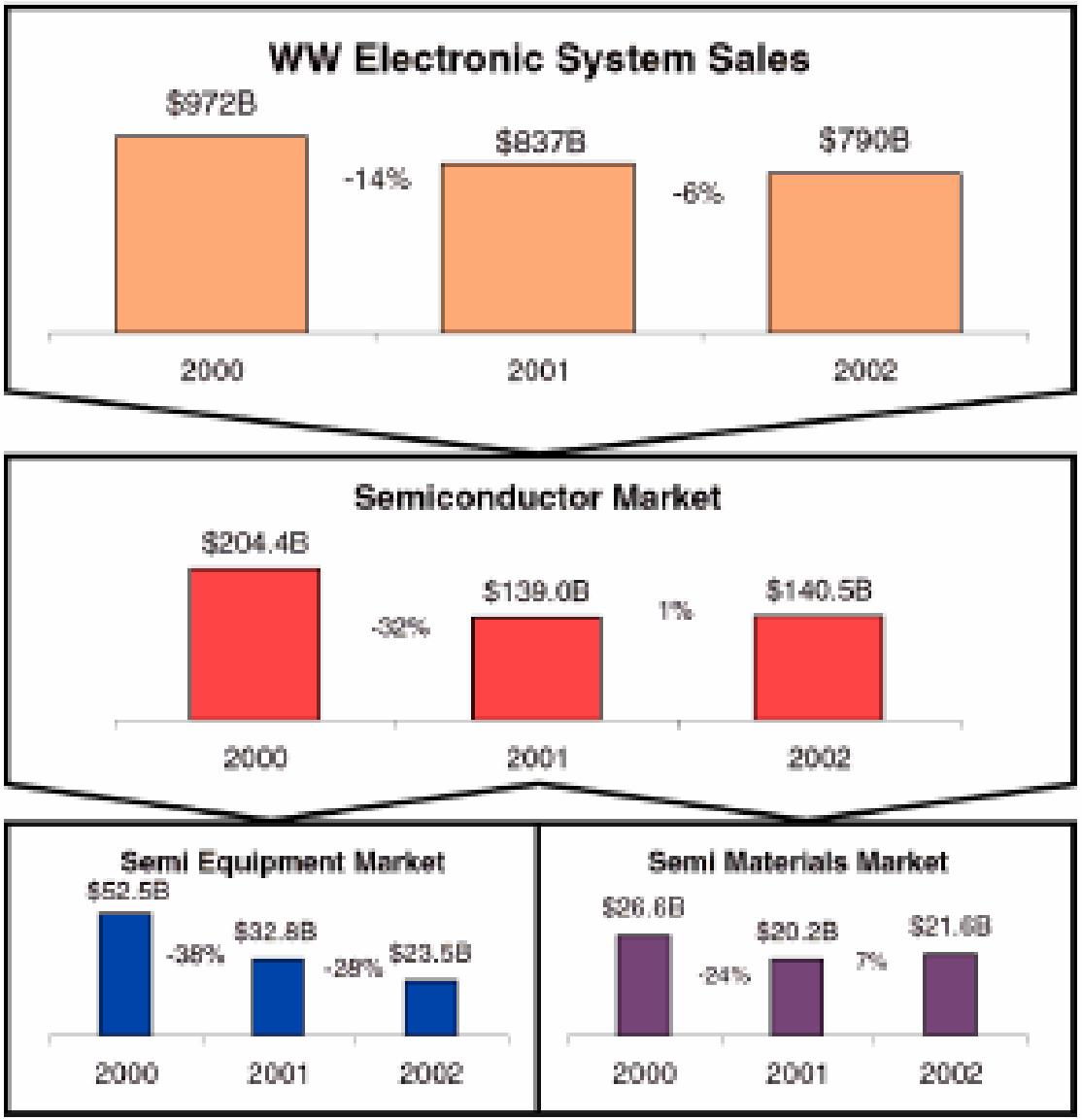


- **The world is increasingly dependent on electronic systems**
- **The "first world" is entirely dependent on electronic systems**
  - **World economy $33.4 trillion http://www.imf.org/**
  - **Electronic systems $1 trillion** Sources: Gartner Group/Dataquest, Rose Associates; January, 2000 http://www.facsnet.org/tools/sci_tech/tech/biz/

Electronic Systems and Semiconductors

- **Electronic systems are entirely dependent on semiconductor components**
  - **Electronic systems $1 trillion**
  - **Semiconductor industry $160 ($141, 147?) billion**
  - **Sources: Gartner Group/Dataquest, Rose Associates; January, 2000 http://www.facsnet.org/tools/sci_tech/tech/biz/**

Electronic Industry Interdependence

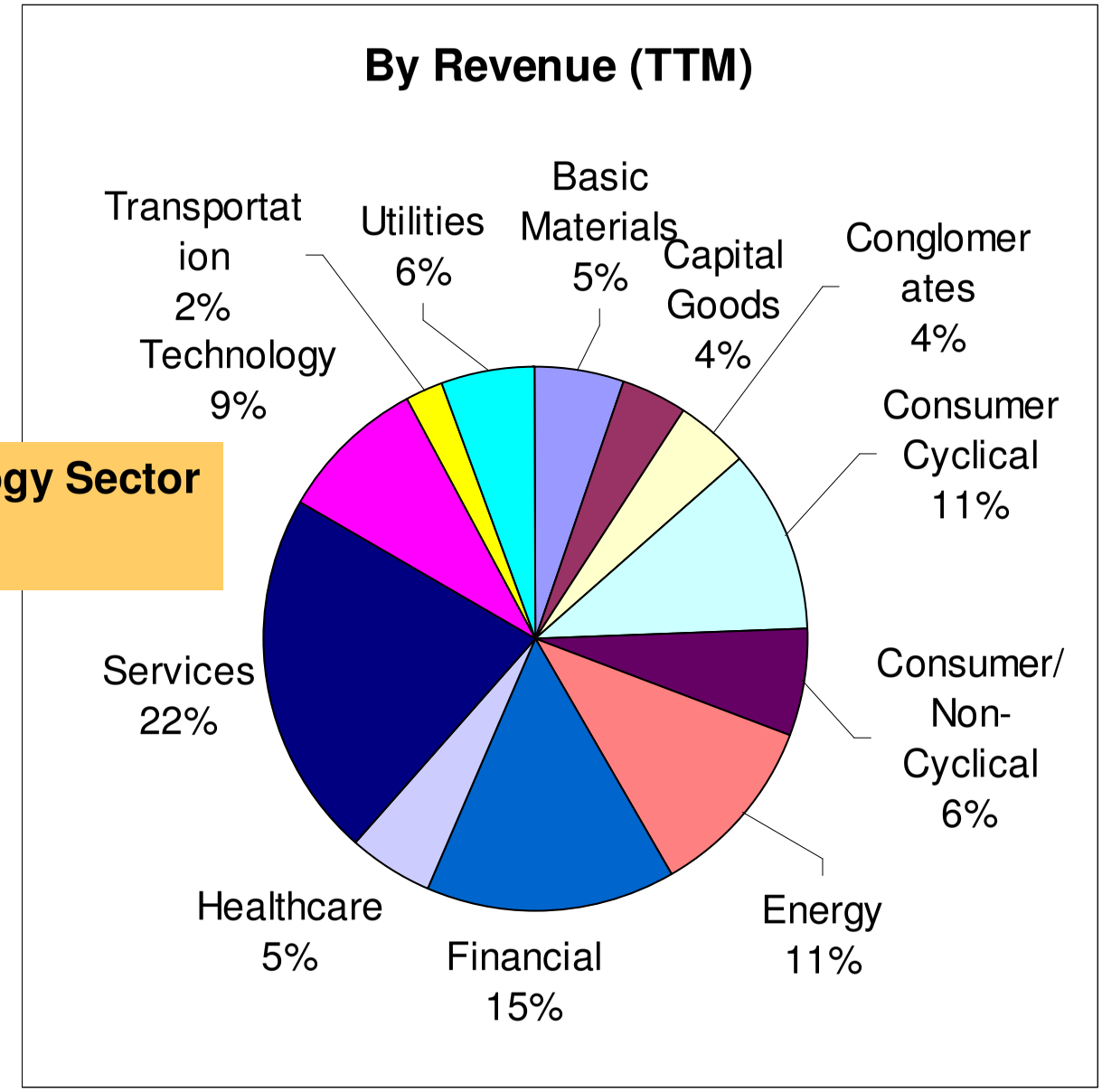


Source: IC Insights, SEMI

An Overview of the Markets

Entire Technology Sector

$1290B



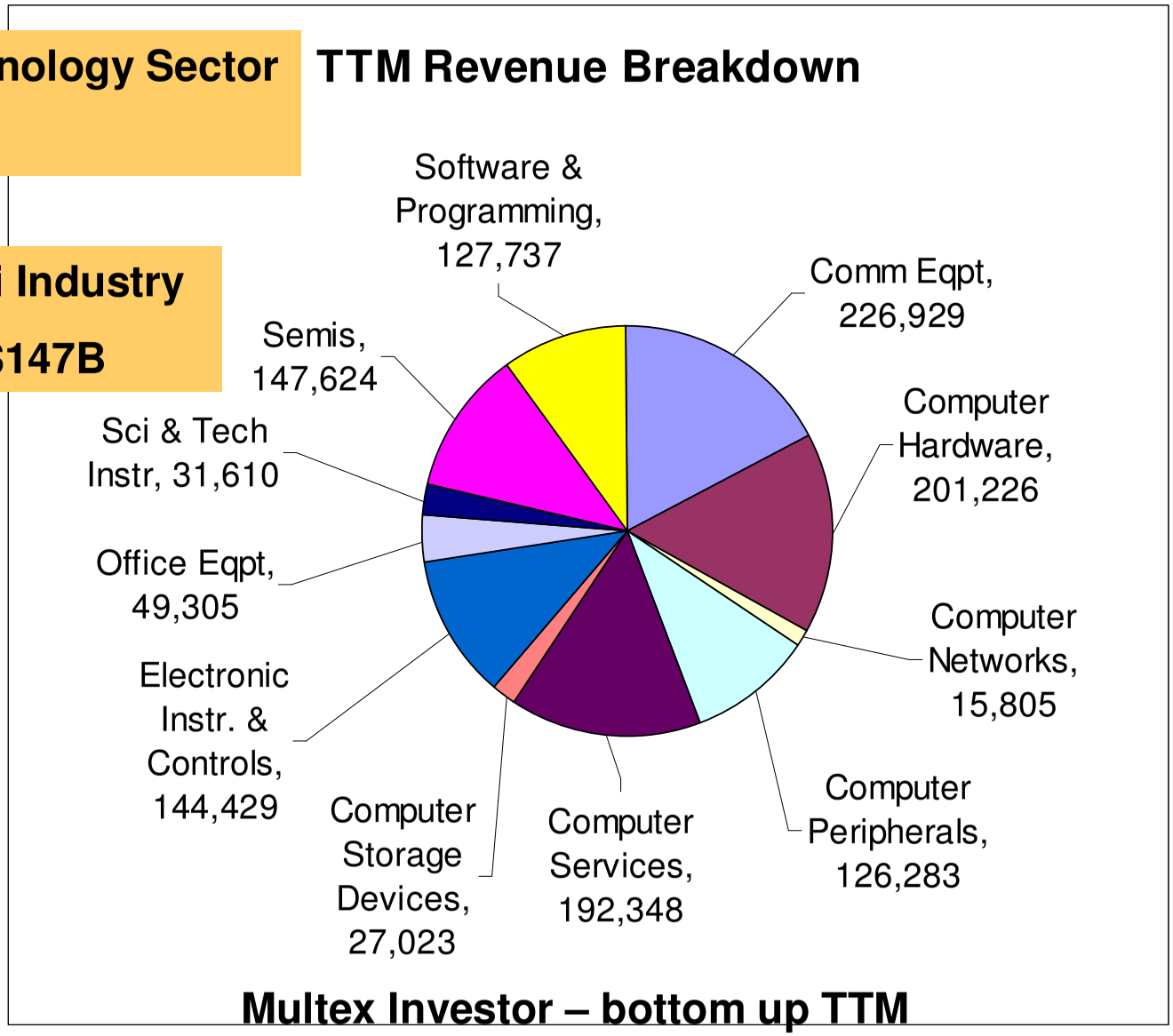
Looking into the Technology Sector

Entire Technology Sector

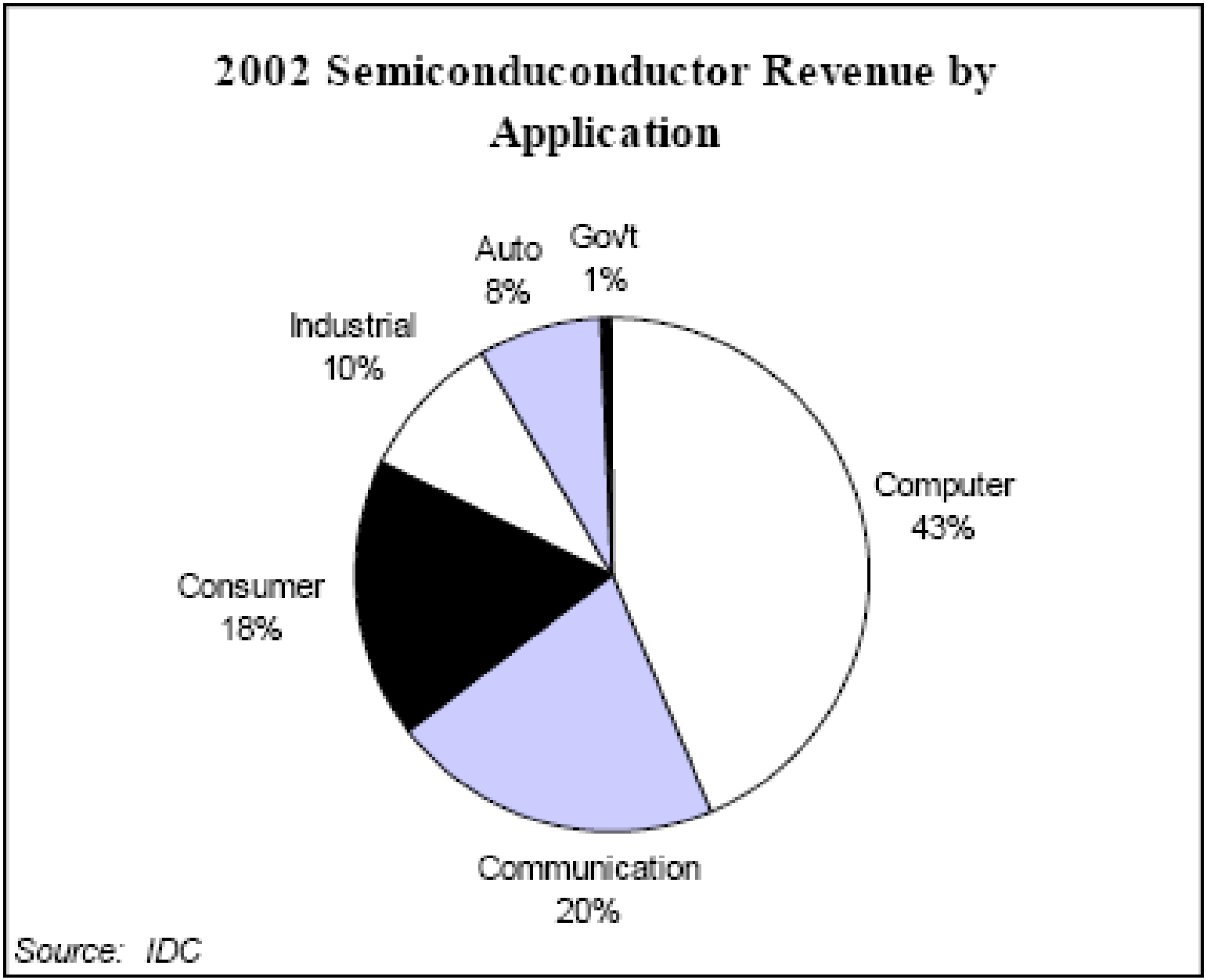
$1290B

Semi Industry

$147B

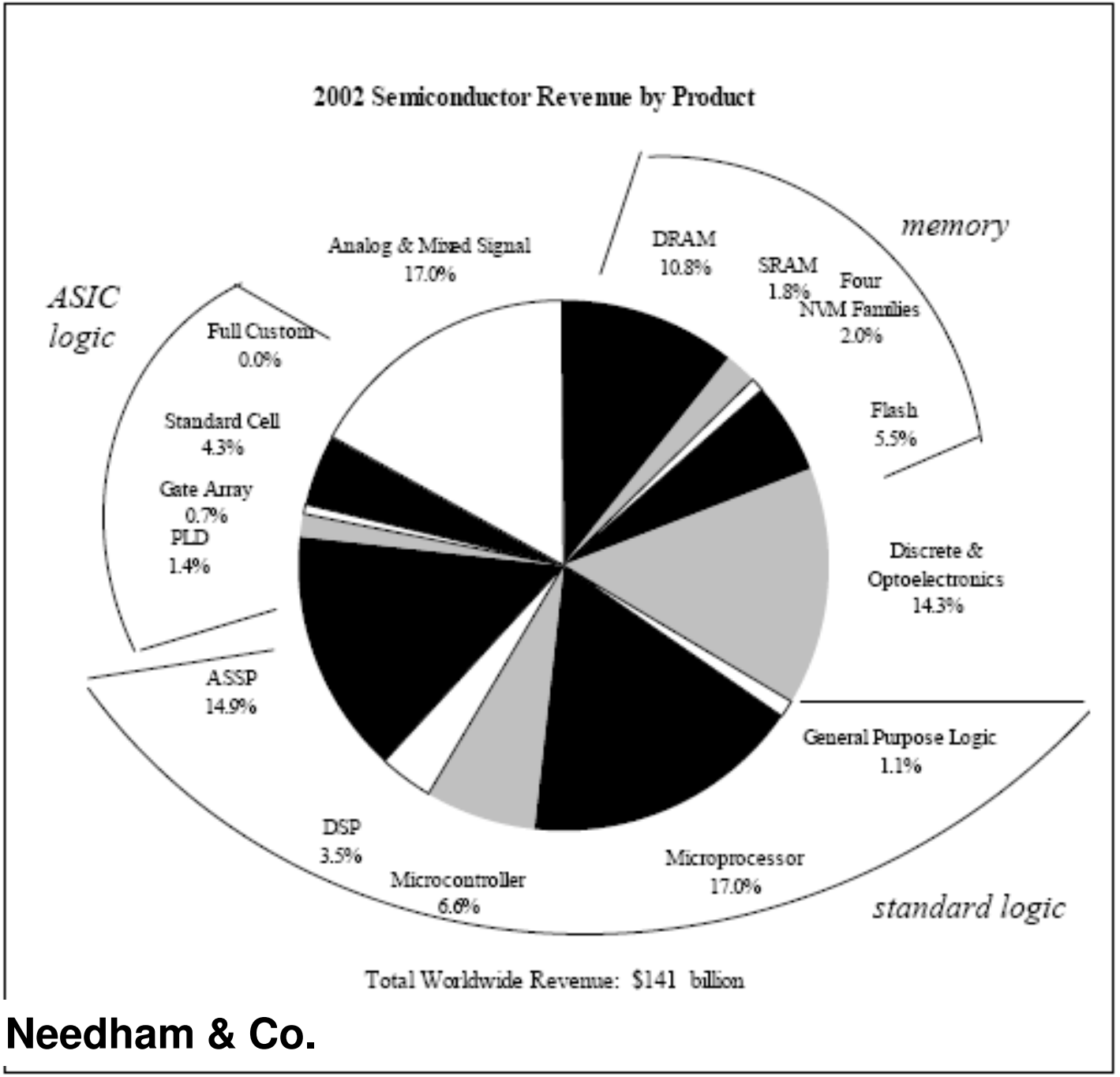


Where does the $141B go?



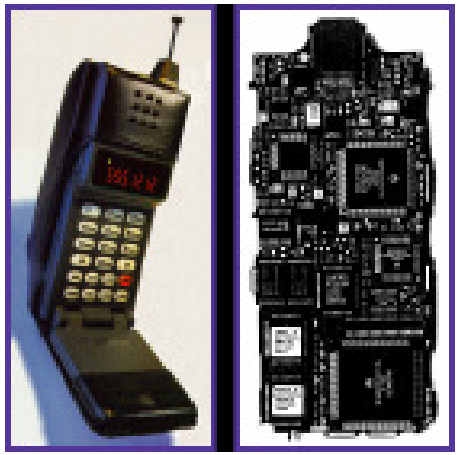
Scovel, 2003, Needham & Co.

Where does the $141B come from?



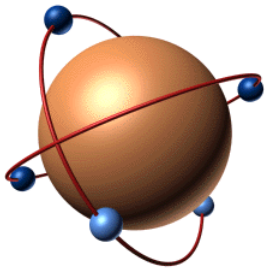
Scovel, 2003, Needham & Co.

Where does CAD fit in?

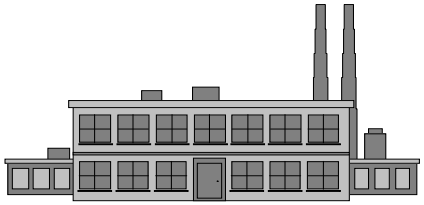


Electronic Systems

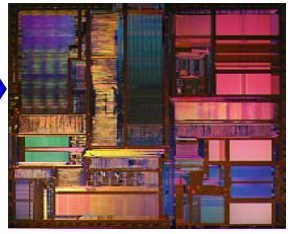
Computer-aided Design



Real World

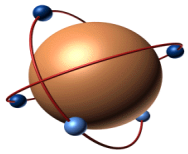


Silicon Foundries



Integrated Circuit

Where does CAD fit in? Everywhere?

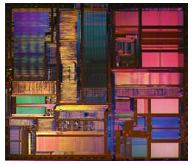


Real World

Speech processing
Signal processing
Performance analysis

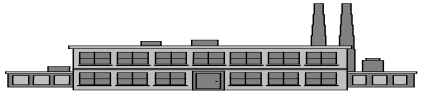
Electronic Systems

System modeling
and synthesis



Semiconductor Industry

Formal verification
Logic synthesis
Place and route
Circuit simulation

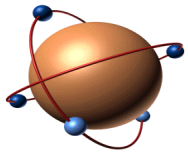


Silicon Foundries

Device simulation
Process modeling

Designer using CAD

Where does CAD fit in? The tools

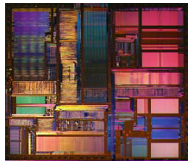


Real World

Matlab
Labview

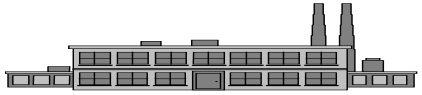
Electronic Systems

SystemC
Metropolis
Ptolemy



Semiconductor Industry

Design compiler
Physical compiler
Apollo



Silicon Foundries

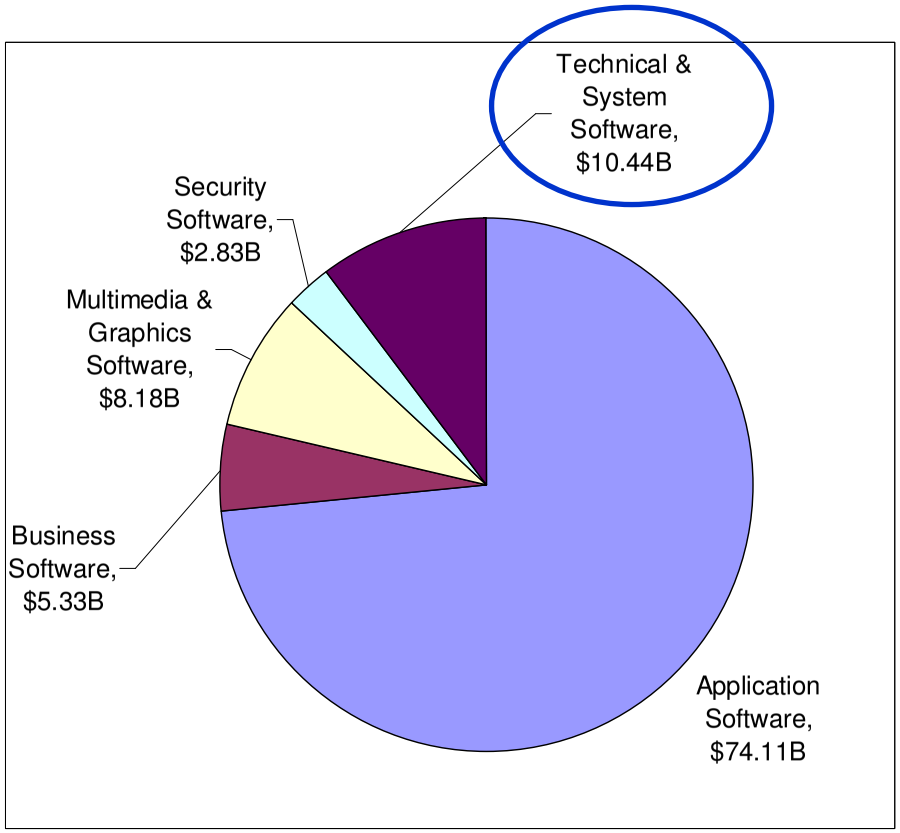
BSIM
Spice
Pisces

Designer using CAD

Where does IC CAD fit in, specifically?

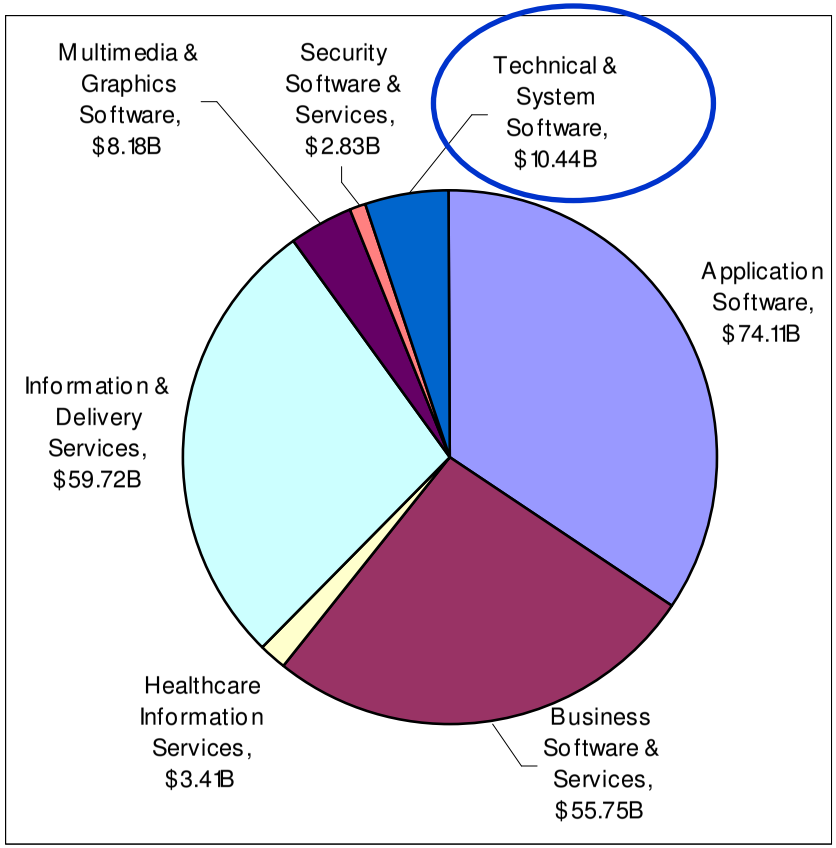
- Computer-aided design (CAD)/Electronic design automation (EDA) enables electronic systems
- CAD principally focuses on support for IC design:
  - ASIC and custom-oriented *design flows*
    - ASIC - 5% of Semi, $7B – e.g. Automatic Target Recognition ASIC in a military system
    - Microprocessors, DSPs, and ASSP - 43%, $60B – e.g. PowerPC, TI TMS320C54, Intel IXP2800
  - Human intensive custom design flows
    - Portions of high performance microprocessors – e.g. Pentium 3
    - FPGA, PLD – 2% of Semi, $3B – e.g. Xilinx 2VP50
  - Human intensive analog design flows
    - Analog ICs – 14% of Semi, $19B
    - Memories – 20% of Semi, $28B
  - Value of CAD to end designer (i.e. customer) depends on the degree to which it significantly eases and automates the design process
  - Revenue of CAD depends on value, size of market served, and *buying behavior*
- Small portion of CAD industry supports board-level design

Software Market Segmentation



Software Market (not incl services)

$100.9B



Software & Services Market

$229.8B

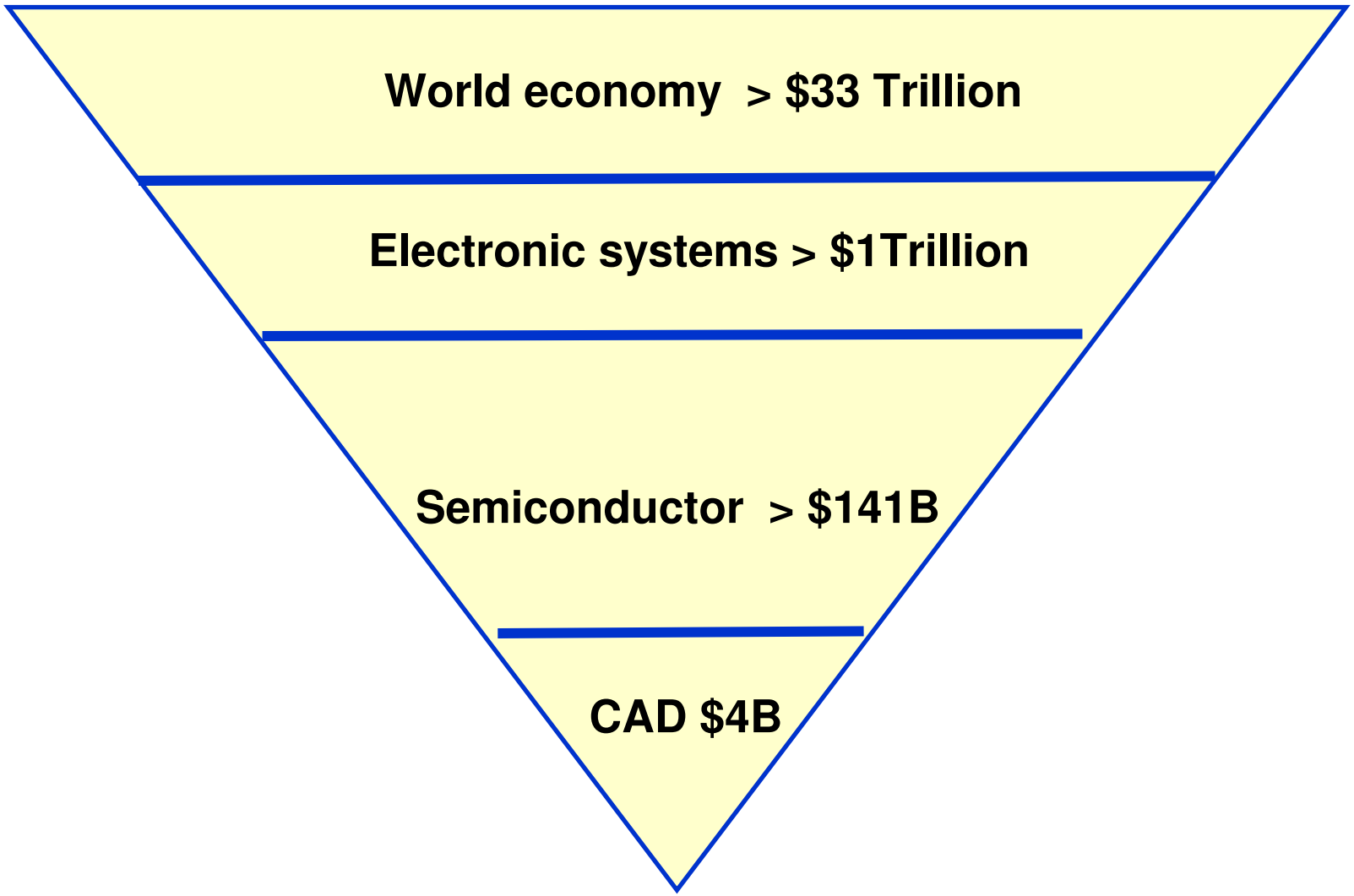
Largest Software Companies - 8/2003

Corporation	Ticker	Market	Rev	Marg	P/E	Price	High	Low
14. Synopsys, Inc	SNPS	$5051	$1106	(16.2)	NM	$65.0	$65.5	$31.8
15. Amdocs Ltd	DOX	$4598	$1427	8.1	40.3	$21.3	$27.3	$5.85
16. Siebel	SEBL	$4595	$1418	(8.2)	NM	$9.30	$12.2	$5.33
17. Check Point Software	CHKP	$3974	$425	58.2	16.6	$16.2	$22.2	$12.6
18. Cadence Design	CDN	$3543	$1136	6.2	50.8	$13.0	$15.6	$8.65
19. Mercury Interactive	MERQ	$3398	$444	15.1	52.7	$39.8	$45.6	$15.2
20. Verisign	VRSN	$3307	$1112	(28.4)	NM	$13.9	$16.1	$3.92

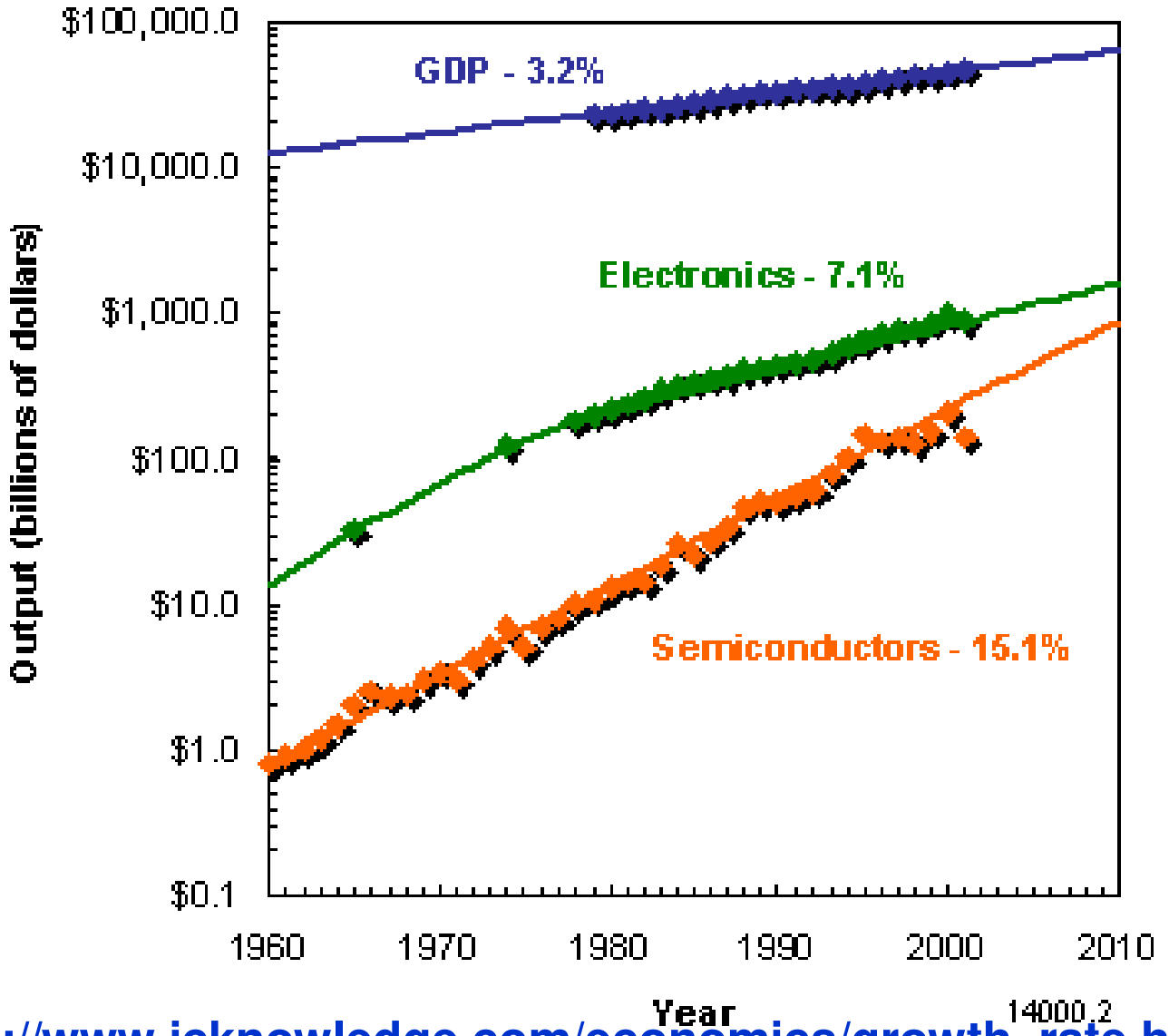
Electronic Systems, Semiconductors and CAD

- **Electronic systems and semiconductor components are entirely dependent on computer-aided design/electronic design automation tools**
  - **Electronic systems $1 trillion**
  - **Semiconductor industry $160B ($141, 147B?)**
  - **EDA industry $3B**
  - **Sources: Gartner Group/Dataquest, Rose Associates; January, 2000 http://www.facsnet.org/tools/sci_tech/tech/biz/**
  - **This is a snapshot – it's important to understand the trends**

The Inverted Pyramid



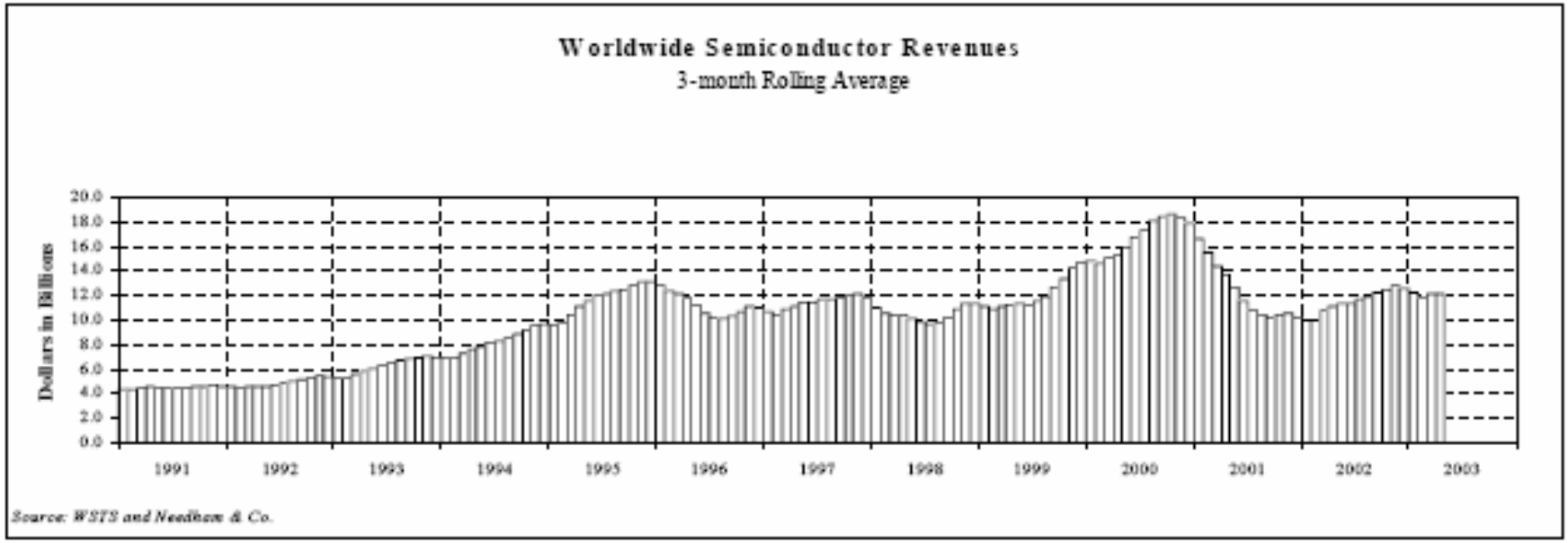
Gross Domestic Product vs ES vs Semi



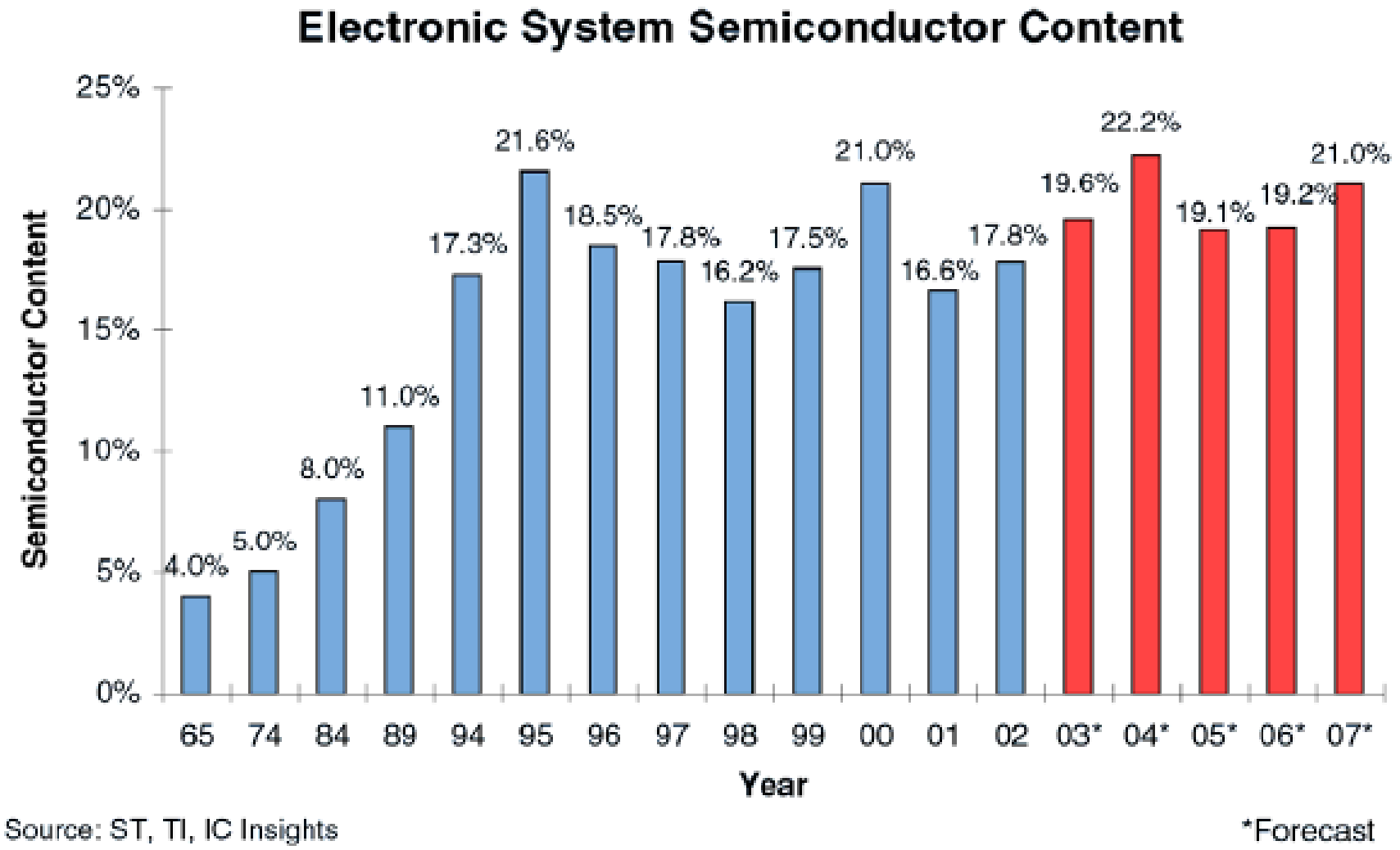
http://www.icknowledge.com/economics/growth_rate.html

What are the trends?

- World economic trends: 4-5% growth rate?
- Electronic system trends: Overall 7% growth rate
- Semiconductor trends: Cyclical semiconductor revenue, overall a 15-16% cumulative growth rate
- Results in electronic systems becoming an increasing portion of world revenue
- Results in semiconductors becoming an increasing portion of electronics systems
- In other words, the world is spending more of their money on electronic systems (e.g. cell phones and playstations) and an increasing amount of the $$ you pay for a Playstation goes to the semiconductor components



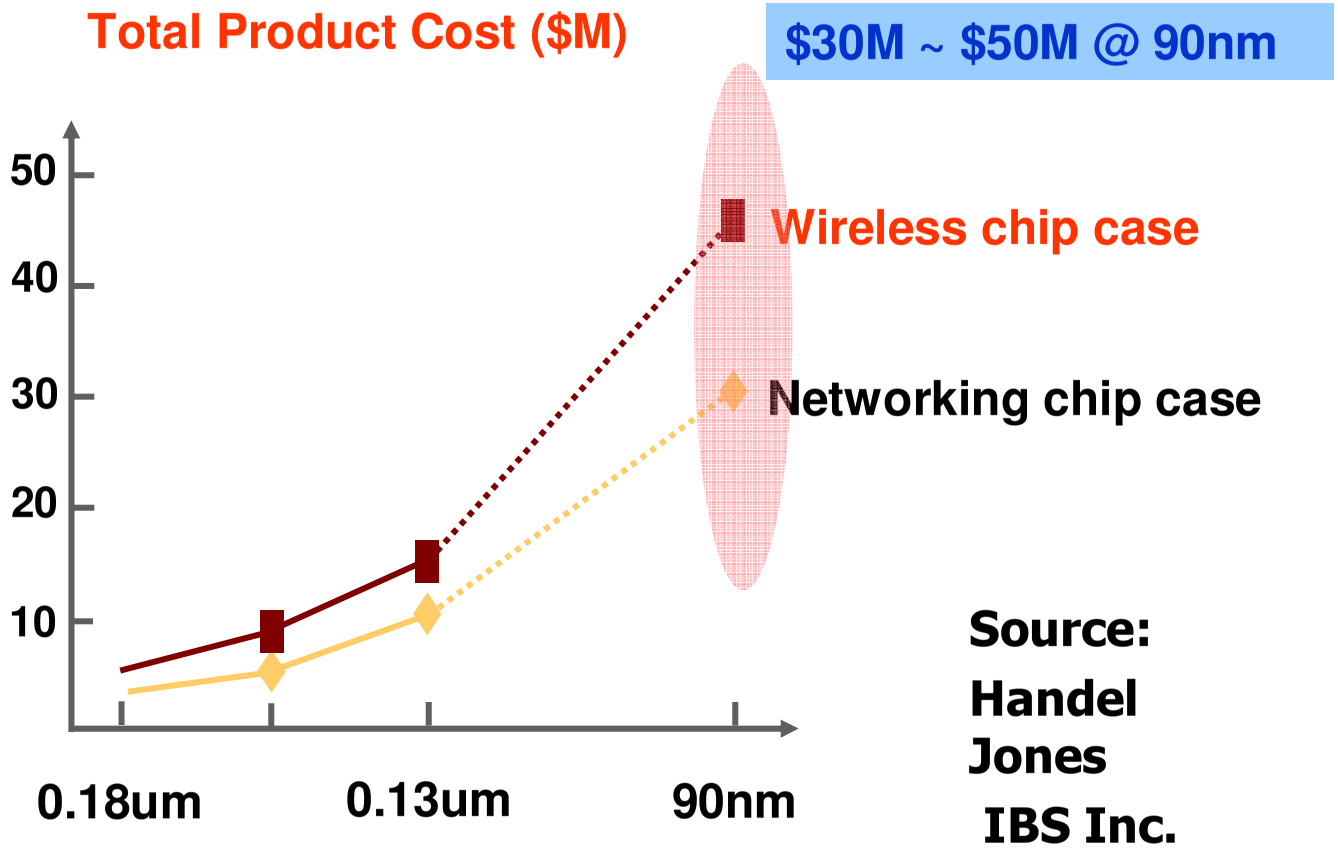
Increasing Semiconductor Content in E Systems



Source: ST, TI, IC Insights

*Forecast

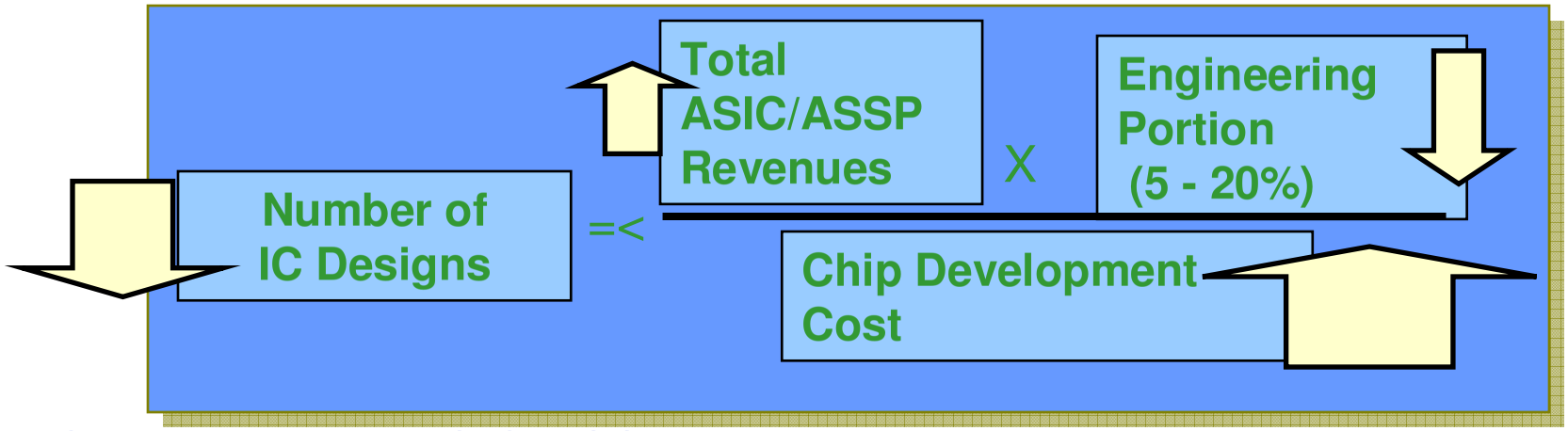
Dramatic Increase in Design Costs



- Going forward, the total cost of design is rising more than 100% per process generation

Handel Jones – IBS, Inc.

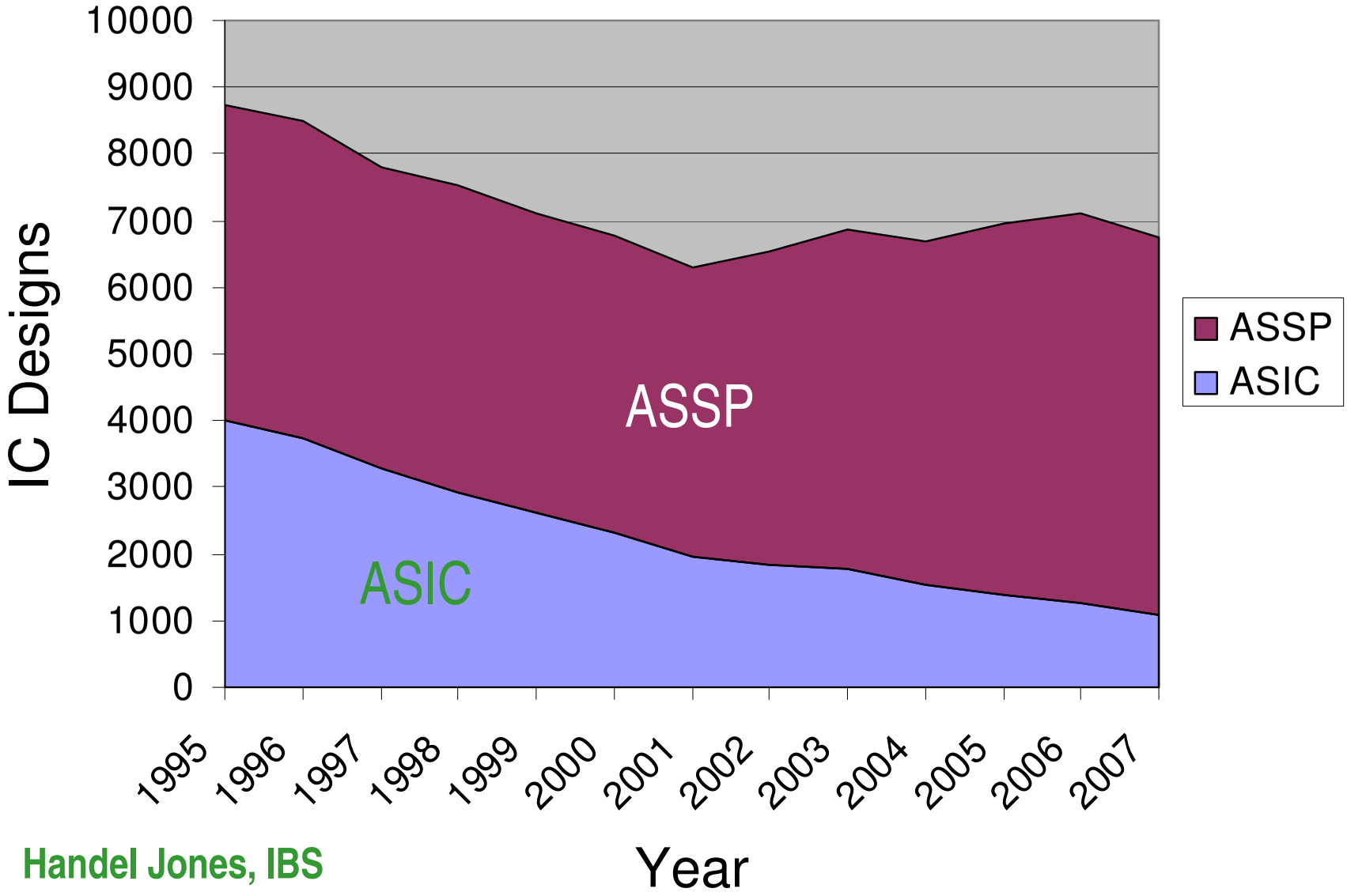
Changing ASIC/ASSP Economics



- Optimistically, ASIC/ASSP revenues growing 10 – 15 % year

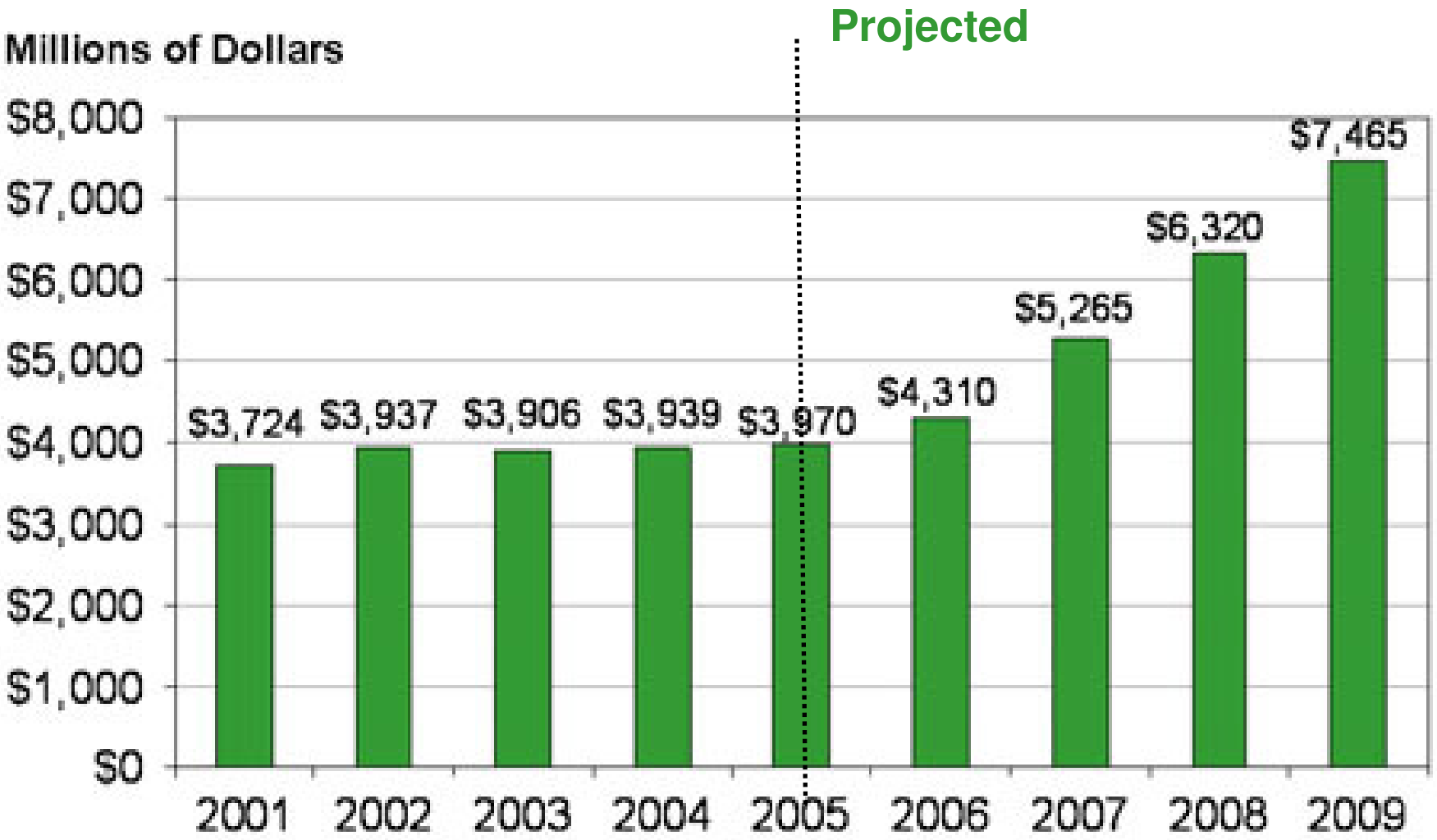
- Engineering portion of budget is supposed to be trimmed every year (but never is)
- Total chip development costs rising 30 – 100% year
- Implies fewer IC designs (doing more applications) - every process generation going forward!!
- Fewer IC design starts means less EDA revenue going forward

Total IC Designs



Handel Jones, IBS
9/23/2002

EDA Industry Trends



G. Smith, Chief EDA Analyst Gartner Dataquest, June 2005

- Increase in revenue based on "Electronic System Level (ESL) design
- http://www.eetimes.com/conf/dac/showArticle.jhtml?articleID=164302406

Review of Trends

- **World economic trends: World GDP ~3% growth rate**
- **Electronic system trends: Overall 7% growth rate**
- **Semiconductor trends: Cyclical semiconductor revenue, overall a 15-16% cumulative growth rate**
- **Results in electronic systems becoming an increasing portion of world revenue**
- **Results in semiconductors becoming an increasing portion of electronics systems**
- **In other words, the world is spending more of their money on electronic systems (e.g. cell phones and playstations) and an increasing amount of the $$ you pay for a Playstation goes to the semiconductor components**
- **But … CAD linked to design *starts* and design *seats* – fewer ASIC design starts means declining revenue**

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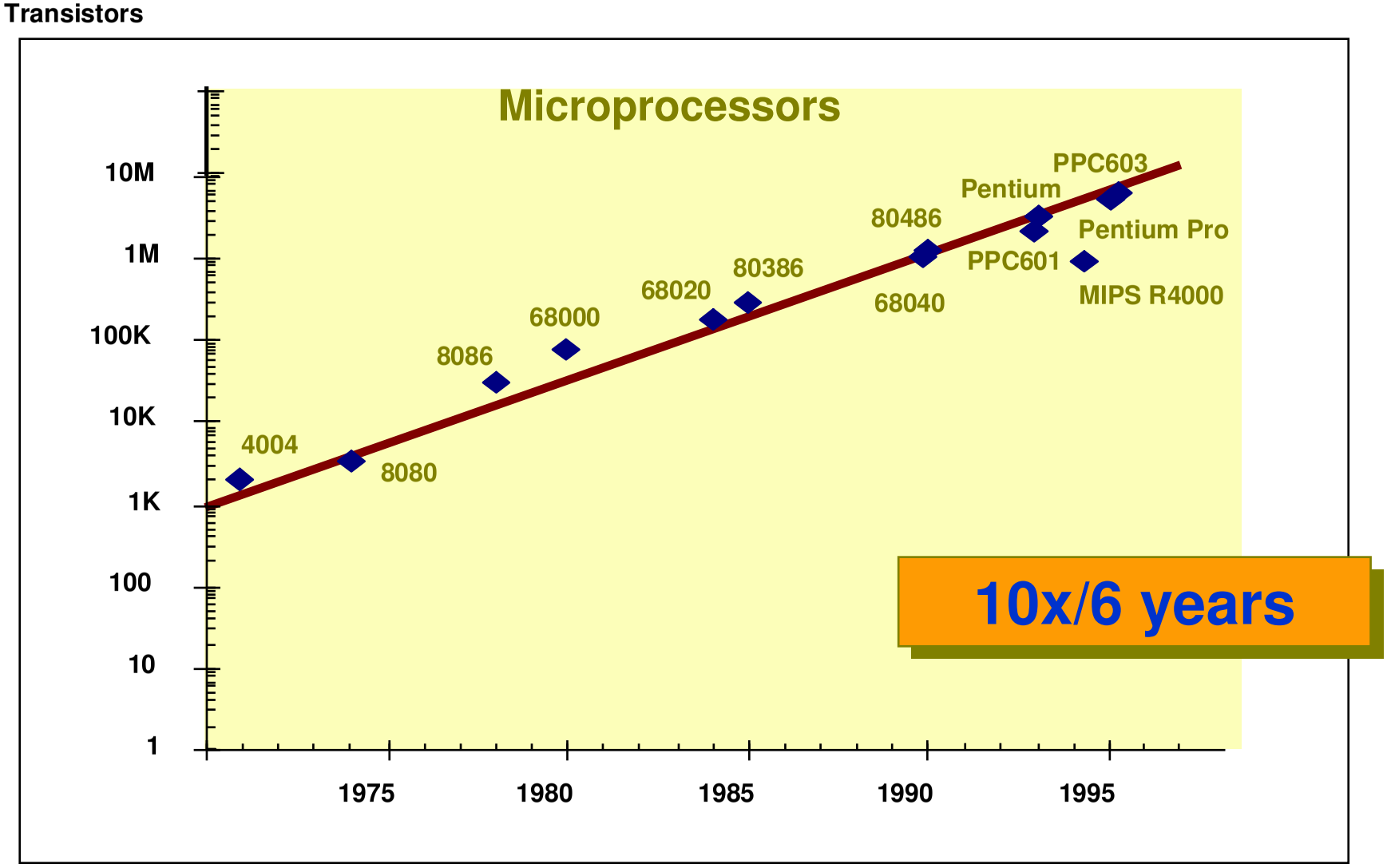
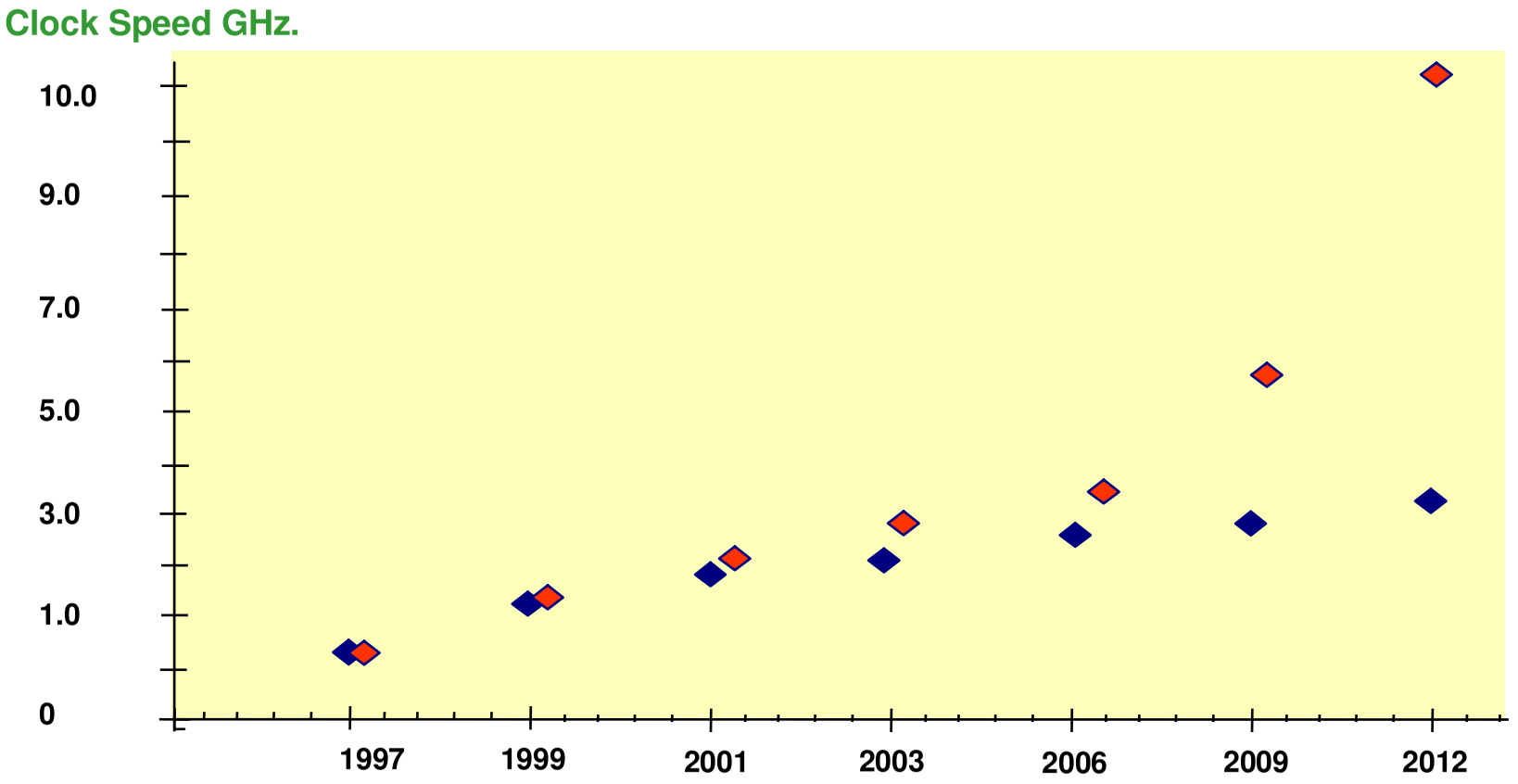
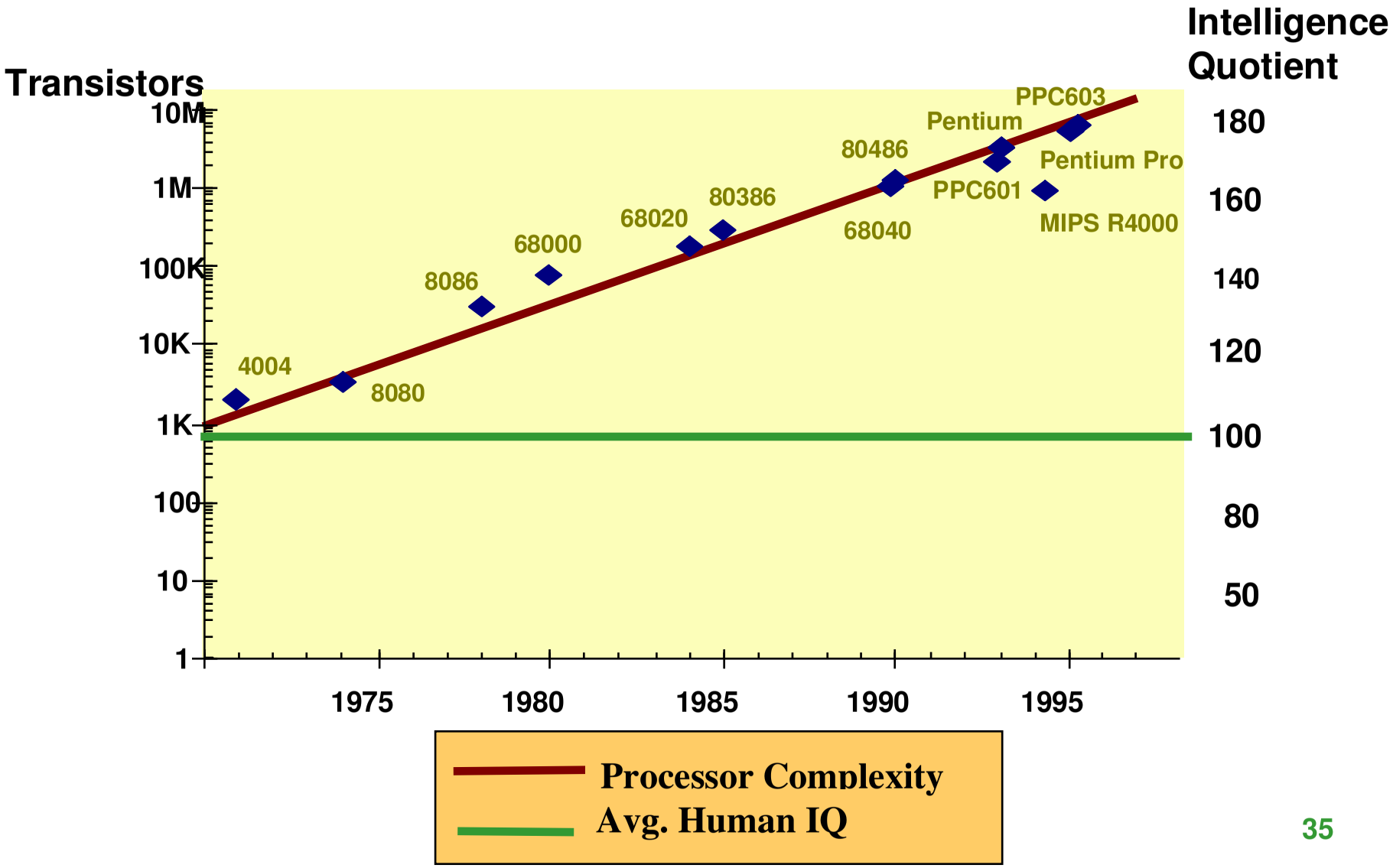
Driving CAD: Moore's Law



NTRS: Chip Frequency (Ghz)



Role of CAD: Helping humans cope

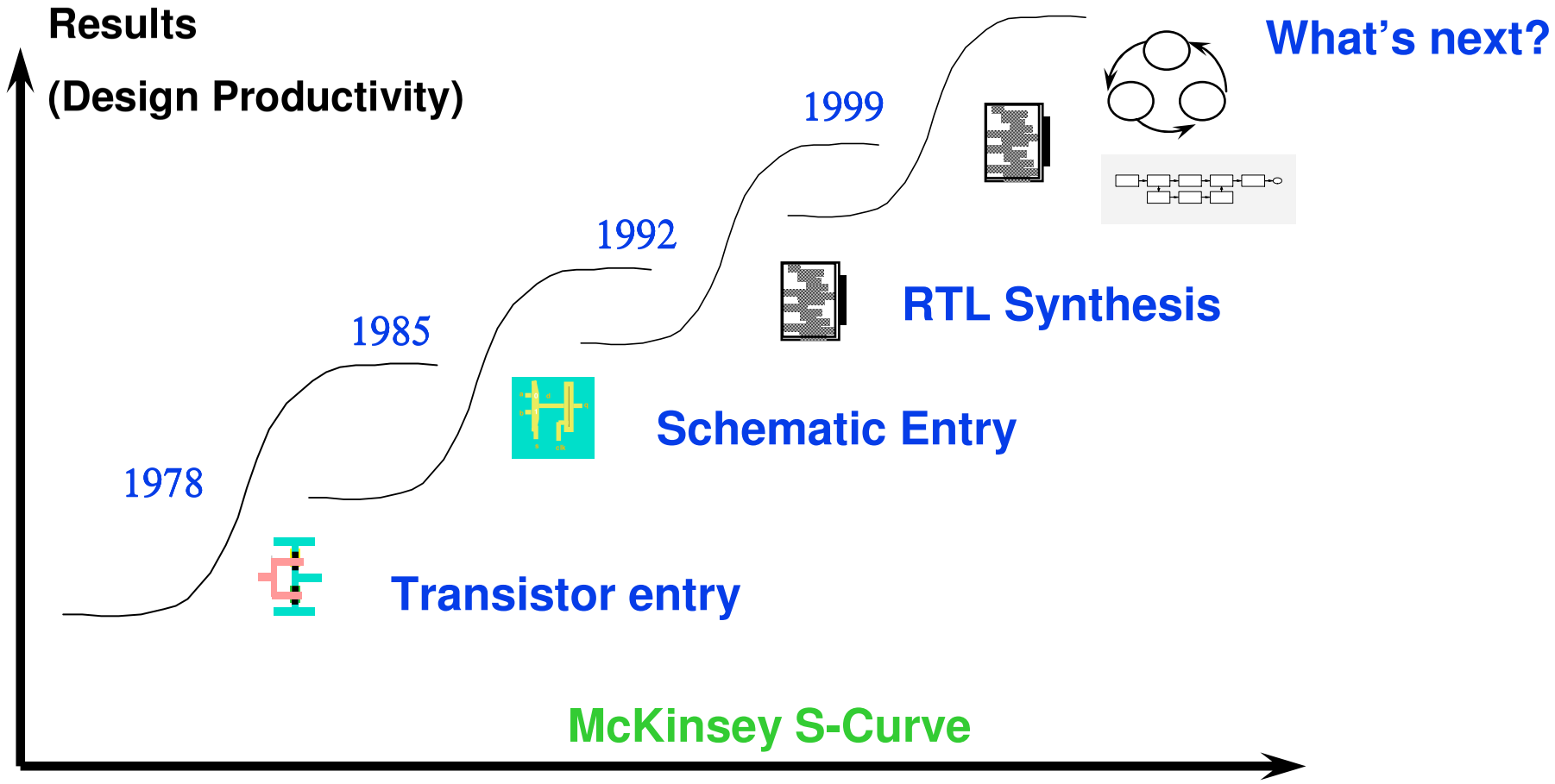


How does Moore's Law drive CAD?

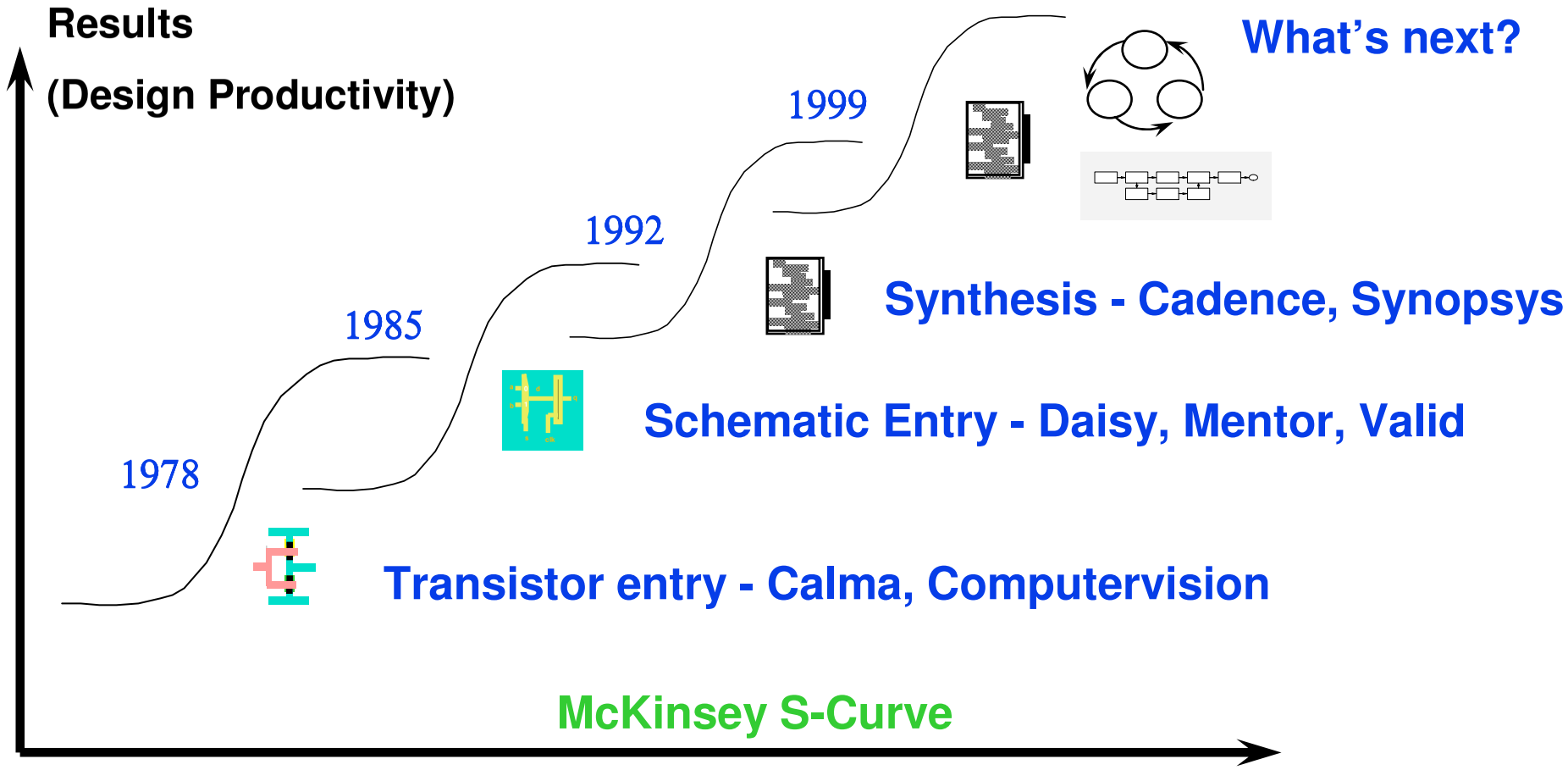
- **Because the capability of integrated circuit technology scales so rapidly, traditionally we have had:**
  - **Exponentially more devices every process generation**
  - **Exponential increases in speed every process generation**
- **Will these trends continue?**

- **After a few process generations we need to do something fundamentally different**
- **CAD is not a field you can relax in!**

Evolution of IC Design

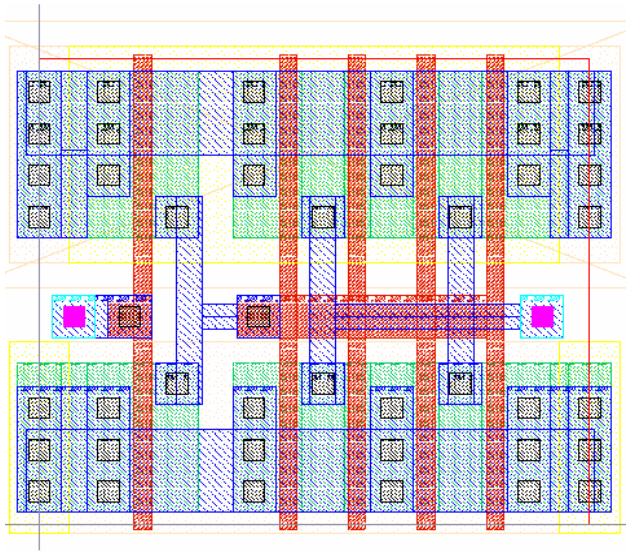


Evolution of the EDA Industry



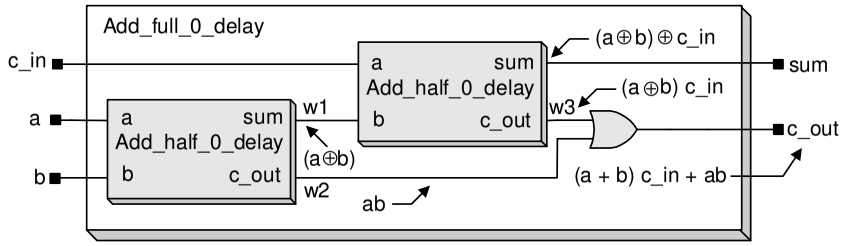
Transistor Era

- Key tools:
  - Transistor-level layout – e.g. Calma workstation
  - Transistor-level simulation – e.g. Spice
  - Bonus: transistor-level compaction – e.g. Cabbage
- Size of circuits: 10's of transistors to few thousand
- Key abstractions and technologies:
  - Transistor-level modeling, simulation
  - Logical gates- NAND, NOR, FF and cell libraries
  - Layout compaction

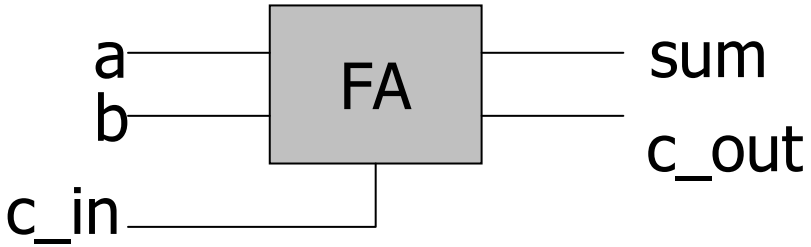


Gate-level Schematic Era

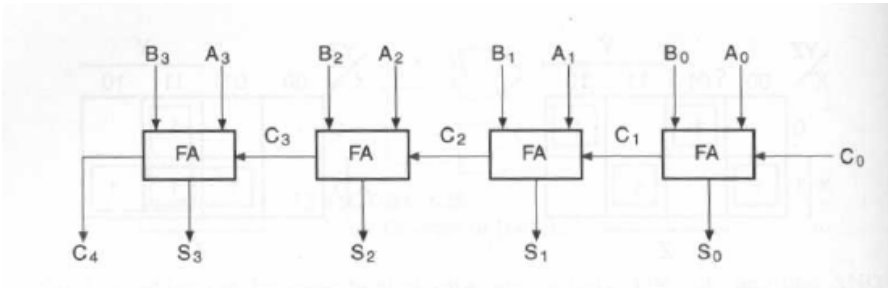
- Key tools:
  - gate-level layout editor – Daisy, Mentor, valid workstation
  - Gate-level simulator
  - Automated place and route



- Size of circuits: 3,000 – 35,000 gates (12,000 to 140,000 transistors)



- Key abstractions and technologies:
  - Logic-level simulation
  - Cell-based place and route
  - Static-timing analysis



Gate level models

J. Christiansen,
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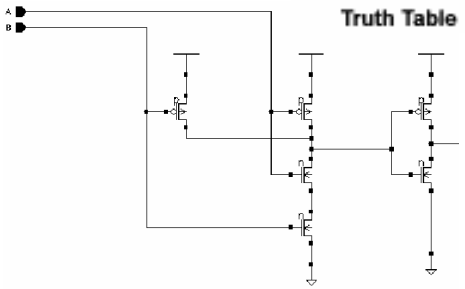
- Border between transistor domain (analog) and digital domain
- Digital gate level models introduced to speed up digital simulation.
- Gate level model contains:
  - Logic behavior
  - Delays depending on: operating conditions, process, loading, signal slew rates
  - Setup and hold timing violation checks
- Gate level model parameters extracted from transistor level simulations and characterization of real gates.

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table

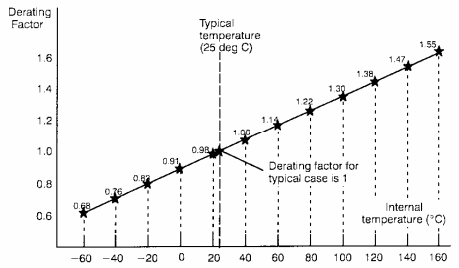


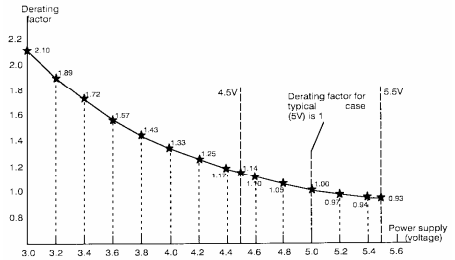
Schematic

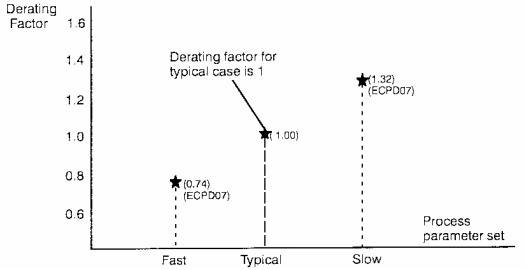
SSAD2 Switching Characteristics
[Delays for typical process, 25.00°C, 2.50V, when t_R and t_F = 0.40ns] [SL(Standard Load) = 0.0081 pF]

Path	Parameter	Delay [ns] SL = 2.00	Delay Equations [ns]		
			Range1*	Range2*	Range3*
A to Y	tPLH	0.13	0.08 + 0.021*SL	0.09 + 0.019*SL	0.09 + 0.019*SL
	tPHL	0.16	0.14 + 0.012*SL	0.15 + 0.009*SL	0.15 + 0.008*SL
	tR	0.13	0.05 + 0.039*SL	0.05 + 0.041*SL	0.04 + 0.041*SL
	tF	0.08	0.05 + 0.014*SL	0.05 + 0.013*SL	0.04 + 0.015*SL
B to Y	tPLH	0.12	0.07 + 0.021*SL	0.08 + 0.019*SL	0.08 + 0.019*SL
	tPHL	0.18	0.16 + 0.012*SL	0.17 + 0.009*SL	0.17 + 0.008*SL
	tR	0.13	0.05 + 0.038*SL	0.05 + 0.041*SL	0.04 + 0.041*SL
	tF	0.07	0.04 + 0.015*SL	0.05 + 0.014*SL	0.04 + 0.015*SL

*Range1 : SL < 3.00, *Range2 : 3.00 ≤ SL ≤ 12.00, *Range3 : 12.00 < SL







RTL Synthesis Era

- Key tools:
  - Hardware-description language simulator – Verilog, VHDL
  - Logic synthesis tool - Synopsys
  - Automated place and route – Cadence, Avant!, Magma
- Size of circuits: 35,000 gates to …?
- Key abstractions and technologies:
  - HDL simulation
  - Logic synthesis
  - Cell-based place and route
  - Static-timing analysis
  - Automatic-test pattern generation

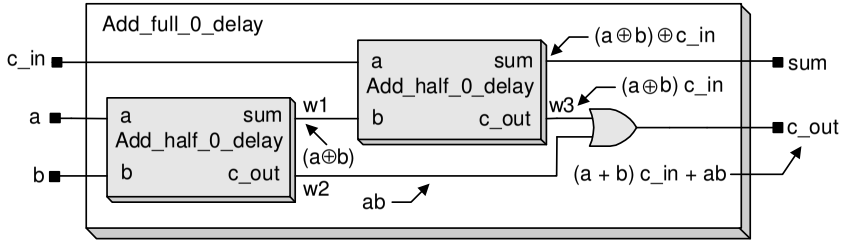
```
module Half_adder (Sum, C_out, A, B);
  output Sum, C_out;
  input A, B;

  xor          M1 (Sum, A, B);
  and          M2 (C_out, A, B);
endmodule
```

```
module Full_Adder (sum, c_out, a, b, c_in);
  output      sum, c_out;
  input       a, b, c_in;
  wire        w1, w2, w3;
  Half_adder  M1 (w1, w2, a, b);
  Half_adder  M2 (sum, w3, w2, c_in);
  or                       M3 (c_out, w2, w3);
endmodule
```

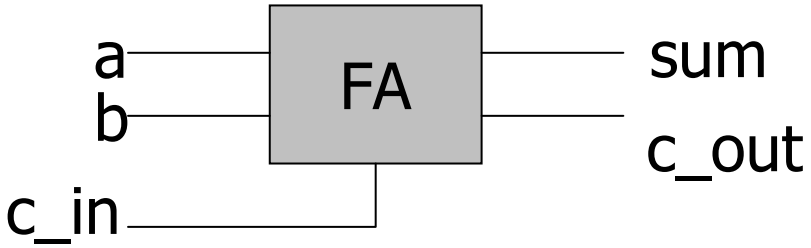
```
module Full_Adder_4 (sum, c_out, a, b, c_in);
  output       [3:0]sum;
  output      c_out;
  input        [3:0] a, b;
  input      c_in;
  wire          c_in2, c_in3, c_in4;
  Full_adder    M1 (sum[0], c_in2, a[0], b[0], c_in);
  Full_adder    M2 (sum[1], c_in3, a[1], b[1], c_in2);
  Full_adder    M3 (sum[2], c_in4, a[2], b[2], c_in3);
  Full_adder    M4 (sum[3], c_out, a[3], b[3], c_in4);

endmodule
```

RTL Synthesis Era

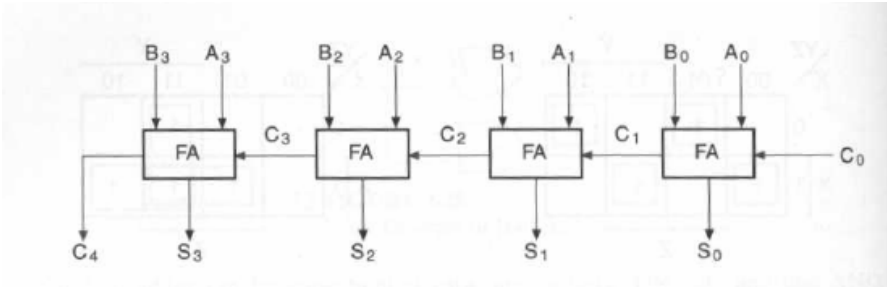
```
module Half_adder (Sum, C_out, A, B);
  output Sum, C_out;
  input A, B;

  xor       M1 (Sum, A, B);
  and       M2 (C_out, A, B);
endmodule
```



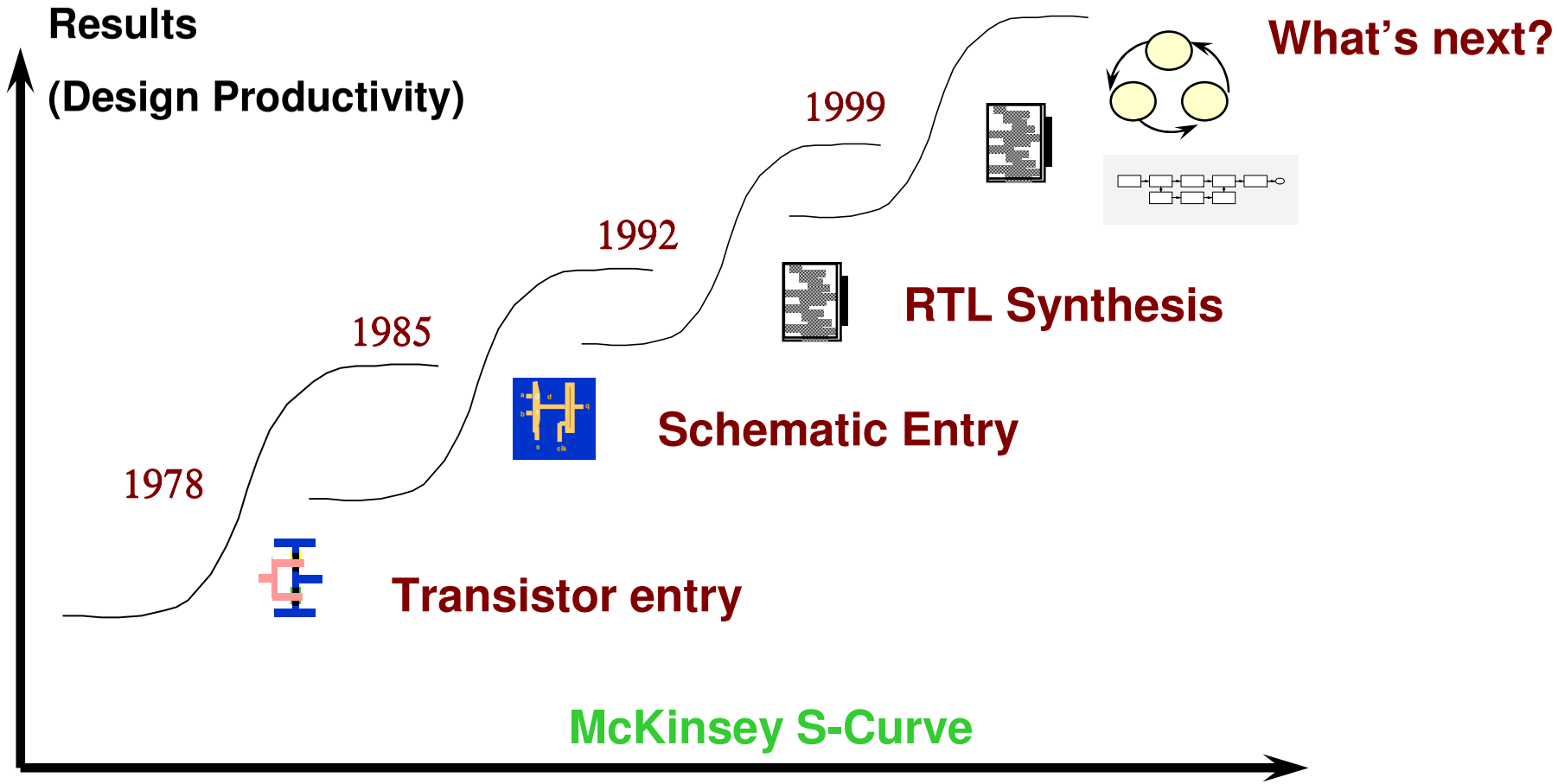

```
module Full_Adder (sum, c_out, a, b, c_in);
  output    sum, c_out;
  input     a, b, c_in;
  wire      w1, w2, w3;
  Half_adder  M1 (w1, w2, a, b);
  Half_adder  M2 (sum, w3, w2, c_in);
  or                    M3 (c_out, w2, w3);
endmodule
```




```
module Full_Adder_4 (sum, c_out, a, b, c_in);
  output      [3:0]sum;
  output      c_out;
  input       [3:0] a, b;
  input       c_in;
  wire        c_in2, c_in3, c_in4;
  Full_adder  M1 (sum[0], c_in2, a[0], b[0], c_in);
  Full_adder  M2 (sum[1], c_in3, a[1], b[1], c_in2);
  Full_adder  M3 (sum[2], c_in4, a[2], b[2], c_in3);
  Full_adder  M4 (sum[3], c_out, a[3], b[3], c_in4);

endmodule
```



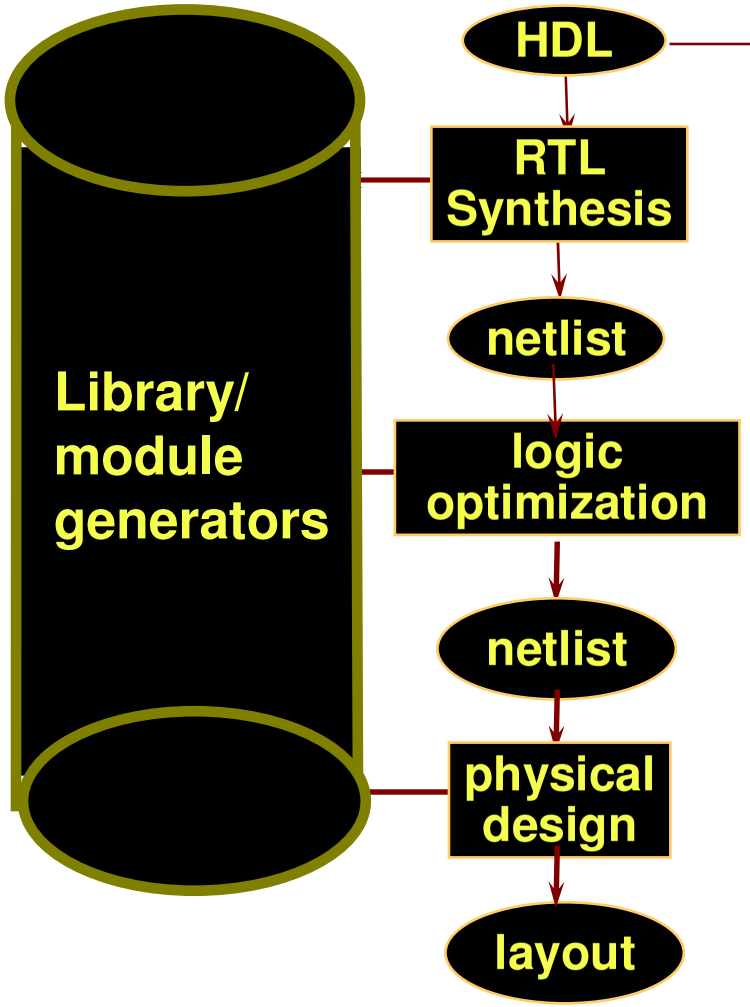
What's after RTL synthesis?



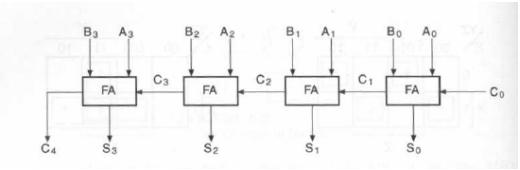
Current Practice: HDL at RTL Level

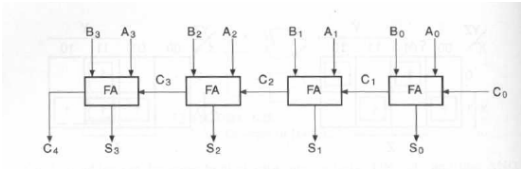
```
module foobar (q,clk,s,a,b);
   input clk, s, a, b;
   output q; reg q; reg d;
always @(a or b or s) // mux
      begin
        if( !s )
          d = a;
        else if( s )
          d = b;
        else
          d = 'bx;
      end // always @ (a or b or s)

always @(clk) // latch
   begin
     if( clk == 1 )
       q = d;
     else if( clk !== 0 )
       q = 'bx;
   end // always @ (clk)

endmodule
```

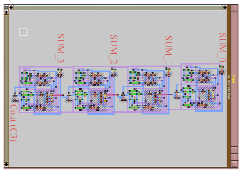
RTL Synthesis Flow




```
module Full_Adder_4 (sum, c_out, a, b, c_in);
  output        [3:0]sum;
  output        c_out;
  input         [3:0] a, b;
  input         c_in;
  wire          c_in2, c_in3, c_in4;
  Full_adder    M1 (sum[0], c_in2, a[0], b[0], c_in);
  Full_adder    M2 (sum[1], c_in3, a[1], b[1], c_in2);
  Full_adder    M3 (sum[2], c_in4, a[2], b[2], c_in3);
  Full_adder    M4 (sum[3], c_out, a[3], b[3], c_in4);

endmodule
```

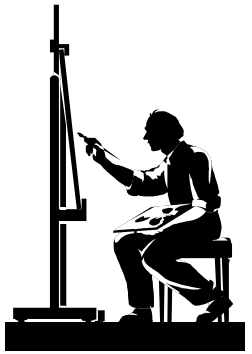






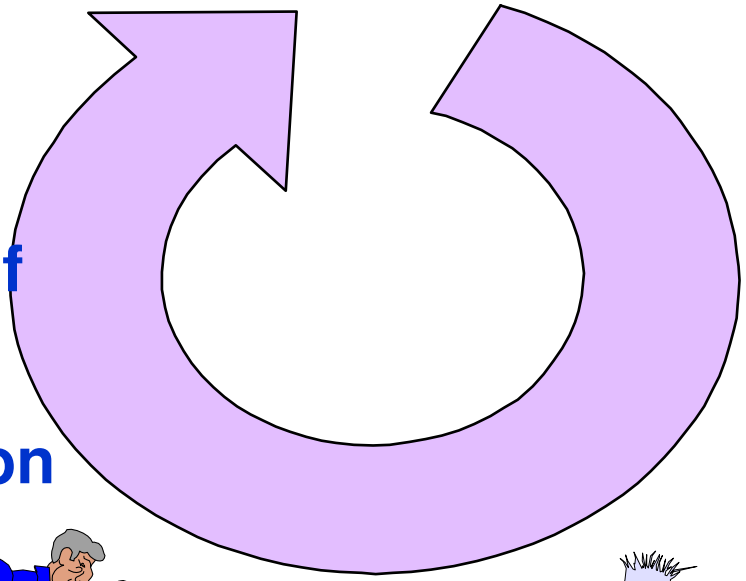
Cover All Aspects of the Design Process

- **Design** : specify and enter the design intent



Verify:

verify the correctness of design and implementation



Implement:

refine the design through all phases

Lecture Overview

- Introduction to Kurt, Sanjit, …. and others
- Education and your future career
- CAD, Semiconductors and the broader economy
- Brief overview of CAD
- Goals of course

Goals of Course

- Help to develop the core competences of a CAD engineer
  - Software expertise
  - Algorithmic facility
  - Domain expertise in ic design
- Communicate the essence of the current IC design flow in a semester
  - Goal: ``If Avanti, Cadence, and Synopsys employees were all abducted by aliens, their software could be recreated by this class.''
- Prepare you for performing publishable research – aim high, a real publication!

Something for Everyone

- **Processing, Devices students – understand the tool flow, examine ways of bridging the gap between processing, design, and CAD**
- **Circuits students – understand how the tools that you will be using for the rest of your life work**
- **CAD students – give you foundation material for the field, prepare you for preliminary examinations**
- **Theory types – understand how algorithms are applied in this algorithm-rich area**

Approach of the Course

- Each week
  - Examine a portion of the IC design flow
  - Identify one or more key problems
  - Formulate the problem mathematically
  - Solve the problem, examining trade-offs between
    - The computational efficiency of the algorithms
    - The quality/optimality of the result
  - Look at contemporary practice
  - See how close the classroom work approaches industrial practice

Course logistics

- EECS 244
- Cory 540A/B, Monday, Wednesday 2:30 – 4:00 PM
- Prof. Kurt Keutzer, Cory 566, Office hour: Monday 4:00– 5:00PM, or by appointment
  - Keutzer at eecs.berkeley.edu
- Prof. Sanjit Seshia, Cory 568 sseshia at eecs.berkeley.edu
- Course reader at Copy Central, 2483 Hearst Avenue, near Euclid
- Recommended book: Logic Synthesis, Devadas, Ghosh, Keutzer – buy from Amazon.com
- Exam 1: 30%
- Exam 2: 30%
- Final project: 40% (20% general content, 10% content in presentation, 10% content in written report)
- No TA for course

- Syllabus, Web page up now

http://www-cad.eecs.berkeley.edu/~keutzer/classes/244fa2005/244fa2005-h6.htm

- The course material will not be hard for you – but the project may be …