

Defect Tolerance on FPGAs

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- FPGAs have inherent capacity for defect tolerance (DT) given regularity + reconfigurability. Since any design uses only a fraction of the FPGA’s resources, DT can increase effective yield. Ideally, exhaustively test FPGA after manufacture to determine defect locations. But getting complete test coverage on FPGAs is difficult because of reconfigurability in routing resources.
- Key Idea: Test only resources used by the specific design at configuration time. Easy since the routing needn’t be modified. But now testing is performed in user’s design cycle, so must be fast!