

Testing in Enhanced Fault Models

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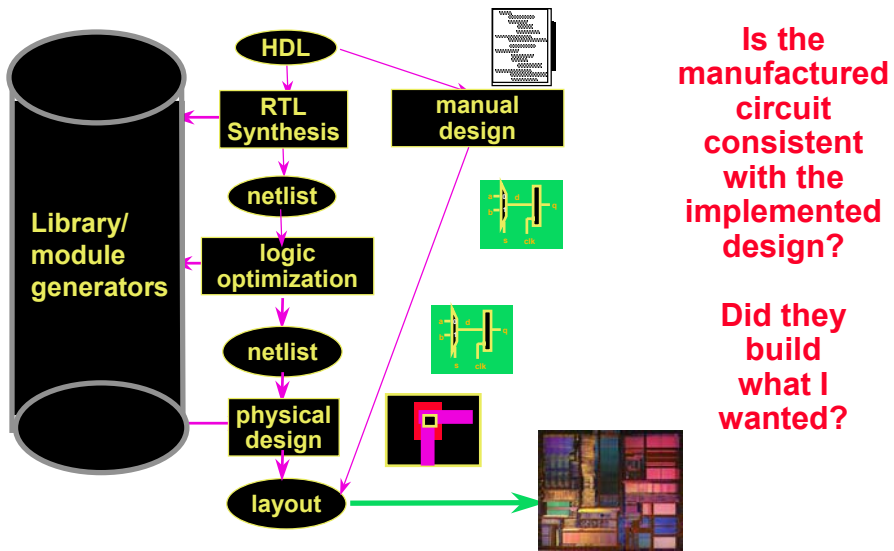
1

Grades for Midterm

- 135 – 147 A+
- 95 – 134 A
- 90 – 95 A-
- 80 – 89 B
- 70 – 79 C
- 60 – 69 D
- <59 F

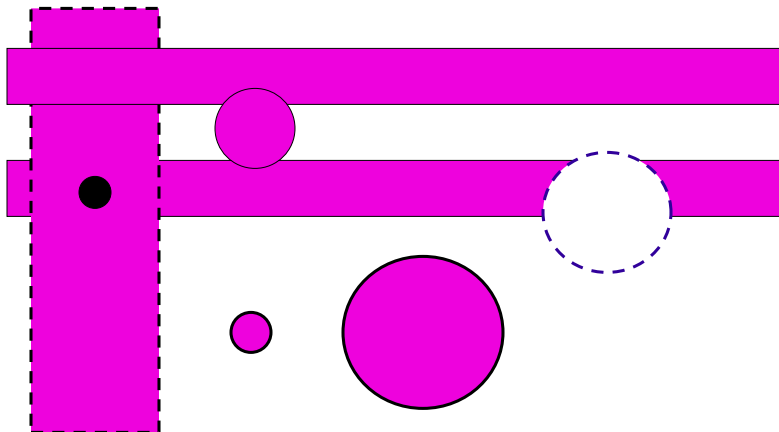
2

Manufacture Verification (Test)



3

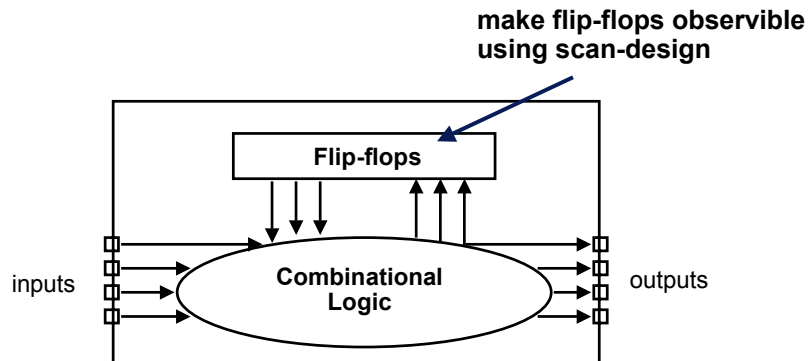
Defect-related Yield Loss



fatal defect types (two types of short circuits, one type of open)

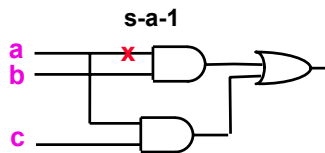
4

Reduce to combinational problem



5

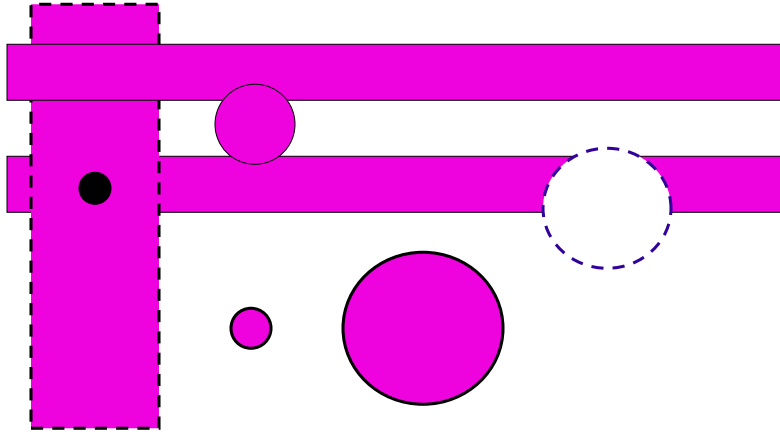
Common fault Model



Single stuck-at fault

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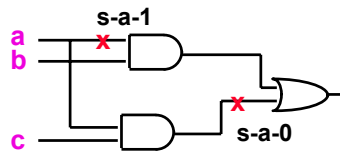
Defect-related Yield Loss



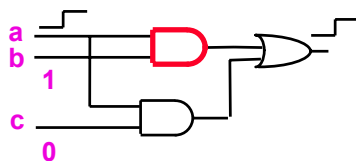
fatal defect types (two types of short circuits, one type of open)
How is this likely to affect circuit?

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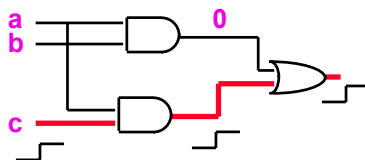
Fault Models - 2



Multiple stuck-at faults



Gate delay fault

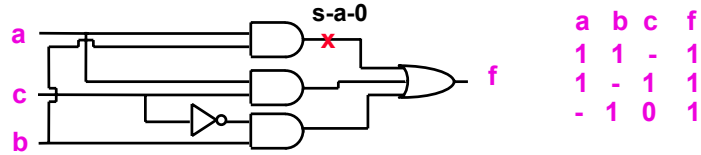


Path delay fault

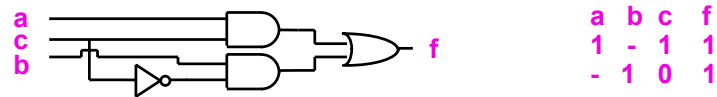
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Redundancy and Testability

If a fault in a circuit is redundant, i.e., there is no test for it



Replace line on which fault resides with a constant 1 (SA1) or 0 (SA0).



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Prime + Irredundant = Testable

A *prime* and *irredundant* cover for a single-output function represents a two-level circuit that is fully testable for all single stuck-at faults.



1	1	0	1
1	-	1	1

non-prime
irredundant
cover

1	1	-	1
1	-	1	1

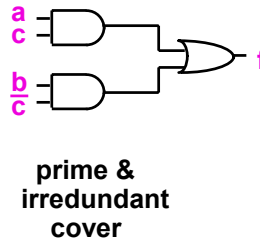
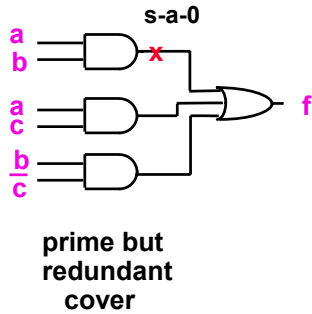
prime &
irredundant
cover

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Correspondence

Primality \Leftrightarrow s-a-1 faults on *AND* gate inputs

Irredundancy \Leftrightarrow s-a-0 faults on *OR* gate inputs



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Multiple-Output Functions

Given the two-output function below

000	01
010	01
100	01
101	01
110	11
111	11

They form a cover

1 1 0	1 1
1 - -	0 1
- - 0	0 1

Prime and irredundant cover

1 1 -	1 1
1 - -	0 1
- - 0	0 1

Is it fully testable for single stuck-at faults?

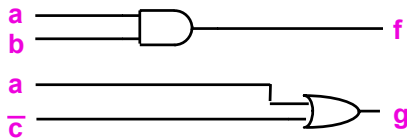
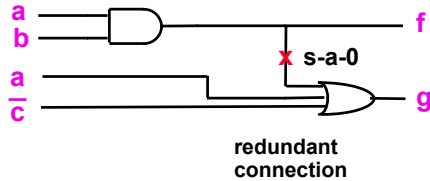
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Multiple-Output Functions - 2

a b c f g

1 1 - 1 1
1 - - 0 1
- - 0 0 1

1 1 - 1 0
1 - 1 0 1
- - 0 0 1



Don't really want just a prime cover

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Testable Multiple-Output Covers

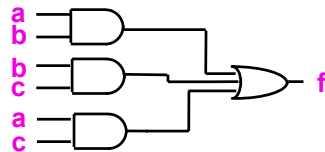
- Modify Quine-McCluskey method
- Generate primes as usual
- During branch & bound covering check selected prime for unnecessary 1's in output part (i.e. check for unnecessary cubes in outputs)
- ⇒ If there are unnecessary 1's, replace prime in current solution with maximally (output) reduced cube.
- Any solution will be fully stuck-at-fault testable

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Multiple Stuck-At Faults

3^K Multifaults

Theorem: The set of tests detecting all single faults in a prime and irredundant single-output two-level circuit detect all multifaults.



$$f = ab + bc + ac$$

s-a-1 on **a** in **ab**

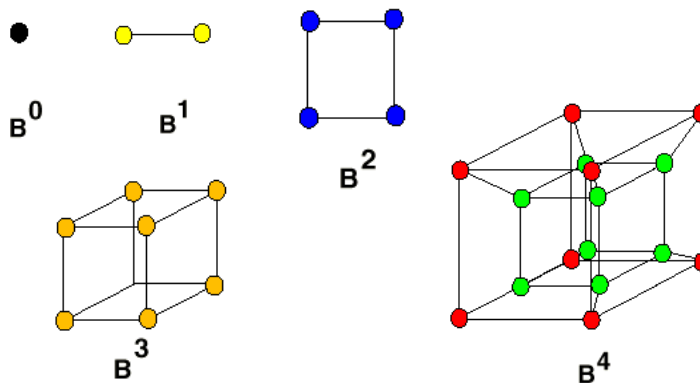
$$f^* = b + bc + ac$$

Additional
s-a-0 on **bc** gives

$$f^* = b + ac$$

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The Boolean n-Cube, B^n

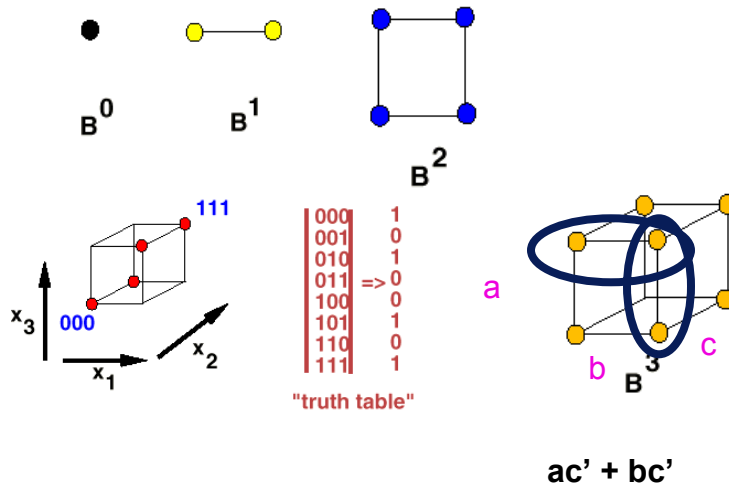


- $B = \{0, 1\}$

- $B^2 = \{0, 1\} \times \{0, 1\} = \{00, 01, 10, 11\}$

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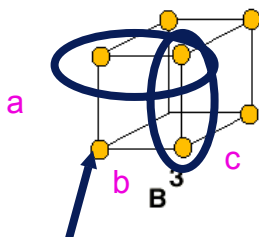
The Boolean n-Cube and a Cover



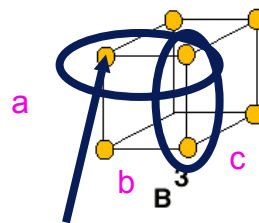
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Primality Test, Redundancy Test

$$F = ac' + bc'$$



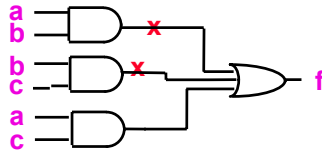
Primality Test
 (Prime literal?)
 a, b , prime should yield
 $F(0,0,0) = 0$



Redundancy Test
 (Redundant Cube?)
 Cube irredundant
 should yield
 $F(1,0,0) = 1$

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Multiple Stuck-At Faults - 1



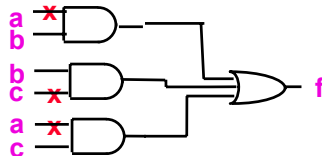
Three cases based on the effect of the multifault:

1. Cubes uniformly removed from f :

s-a-0 test for any removed cube will detect multifault

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Multiple Stuck-At Faults - 2



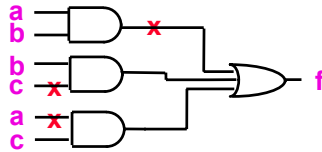
Three cases based on the effect of the multifault:

2. Cubes uniformly raised/expanded in f :

**s-a-1 test for some removed literal in cube
(primality test) will detect multifault**

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Multiple Stuck-At Faults - 3



Three cases based on the effect of the multifault:

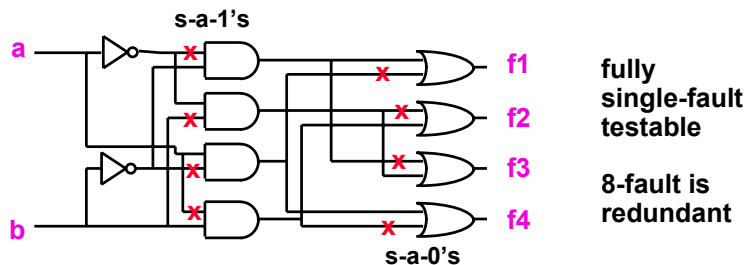
3. Some cubes removed, some raised:

- s-a-1 test for some removed literal in unremoved cube will detect multifault.
- Why must there be at least one such literal in one such cube?

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Multiple-Output Circuits

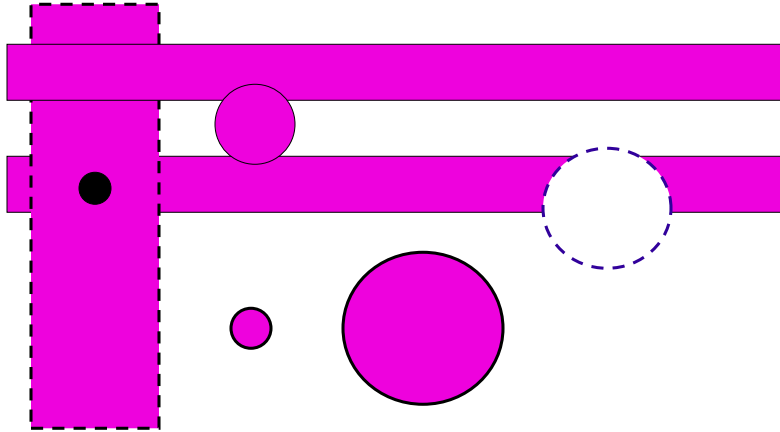
Theorem does not generalize to multi-outputs



Need to implement each single-output “cone” as prime and irredundant circuit for full multifault testability

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Defect-related Yield Loss

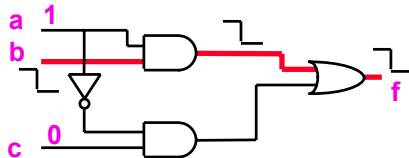


fatal defect types (two types of short circuits, one type of open)
How is this likely to affect circuit?

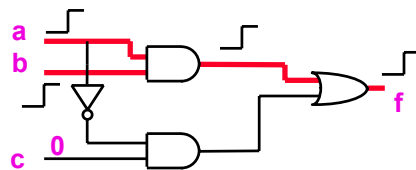
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Enhanced Model: Path Delay Faults

Need to propagate transition down the path that is to be tested



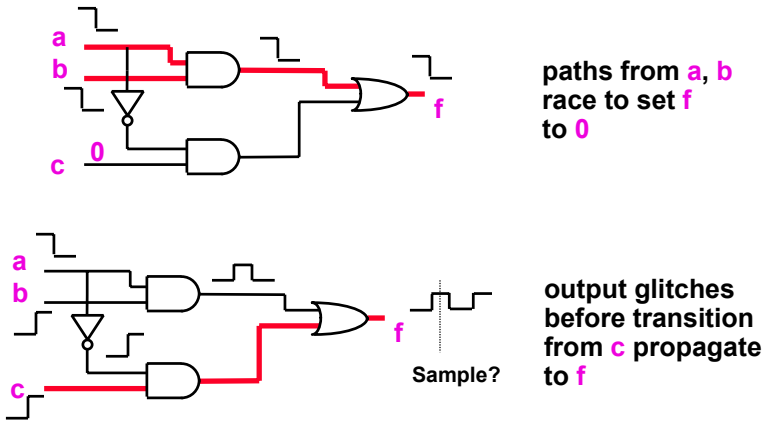
path from **b** to **f**
is tested



paths from **a, b**
to **f** are tested

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Robust/Hazard Free Testing

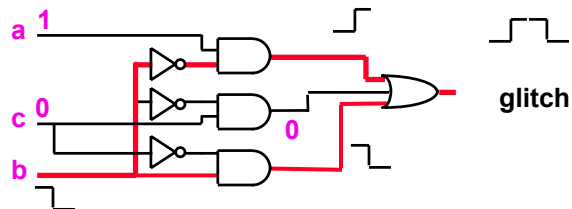


Have to avoid races and hazards \Rightarrow robust testing

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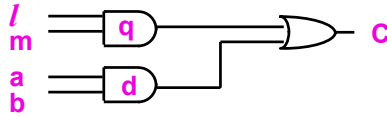
Path Delay Fault Testability

Not all paths in a prime and irredundant two-level circuit are robustly testable



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Definitions



A path Π in circuit C is associated with a literal l in cube q

A relatively essential vertex of a cube q is a *minterm* that is not in any other cube of C but is in q

$l m!ab$ is a *relatively essential vertex* of q above

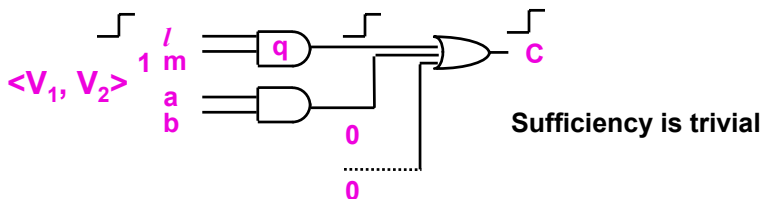
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Testability Conditions

Theorem: (Devadas & Keutzer) Let C be a single-output circuit. Let Π be a path in C that starts with l in cube q .

There exists a hazard-free robust delay fault test for Π if and only if:

- 1) There exists a vertex V_2 that is a relatively essential vertex of q and
- 2) Vertex V_1 distance-1 from V_2 in l is in the OFF-set of C .

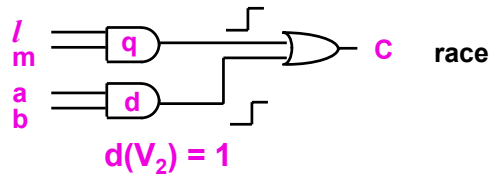


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Necessity

Suppose $\langle W_1, V_2 \rangle$ is a delay-fault test for Π .

Suppose V_2 is not a relatively essential vertex of q .



So V_2 has to be a relatively essential vertex of q .

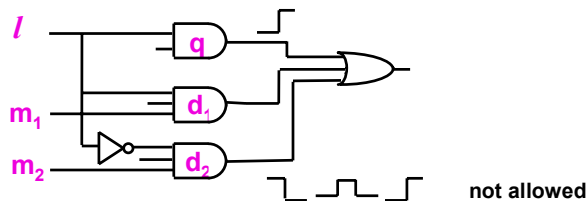
Clearly W_1 has to be in the OFF-set of C .

But do W_1 and V_2 have to differ only in l ?

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Necessity - 2

If W_1 and V_2 are not distance-1 in l we can construct a V_1 and V_2 distance-1 in l that are a delay fault test for Π .

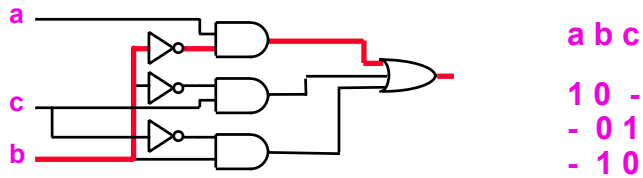


Need some literal $m_i \in d_i$ such that $m_i = 0$ for both W_1 and V_2 . Else glitch would invalidate test.

Just arbitrarily set remaining literals in W_1 other than l to values in V_2 .

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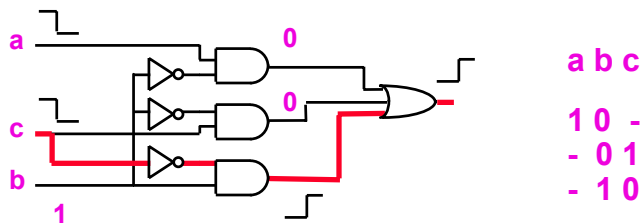
Example - I



Relatively essential vertex of cube $a!b\ 10-$ is 100
 But 110 (distance-1 from 100 in b) is in the ON-set
 Therefore, there is no robust path delay fault test
 for this path

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Example - II



$\langle 111, 010 \rangle$ is a robust path delay fault test

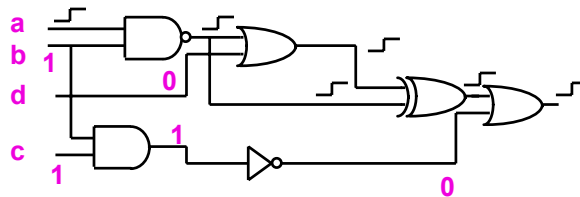
Can construct distance-1 test by setting
 literals in V_1 other than c to values in V_2

Obtain $\langle 011, 010 \rangle$, which is also a robust test

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Testability of Multilevel Circuits

Were able to obtain necessary and sufficient conditions for robust path-delay-fault and multi-fault testability based on *primality* and *irredundancy* for two-level circuits

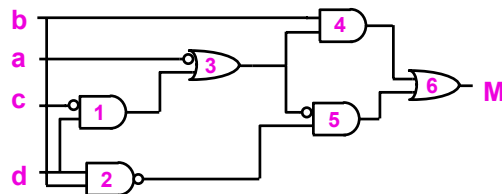


What about multilevel circuits?

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Equivalent Normal Form

ENF is a two-level representation of a multilevel circuit

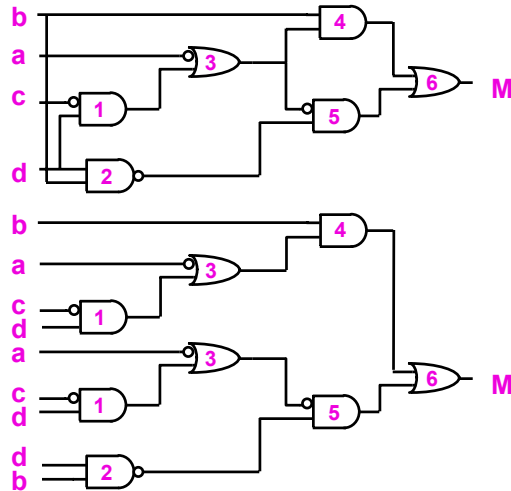


$$\begin{aligned}
 E_M = & b_{4,6} \bar{a}_{3,4,6} + b_{4,6} \bar{c}_{1,3,4,6} d_{1,3,4,6} \\
 & + a_{3,5,6} c_{1,3,5,6} \bar{d}_{2,5,6} + a_{3,5,6} c_{1,3,5,6} \bar{b}_{2,5,6} \\
 & + a_{3,5,6} \bar{d}_{1,3,5,6} \bar{d}_{3,5,6} + a_{3,5,6} \bar{d}_{1,3,5,6} \bar{b}_{2,5,6}
 \end{aligned}$$

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Computing the ENF

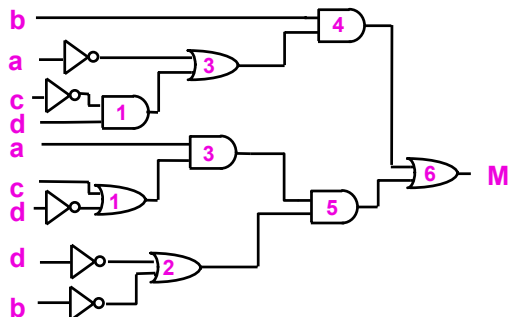
Make the circuit fanout-free internally



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Computing the ENF - 2

Push inverters to primary inputs



There is a one-to-one correspondence between paths in above circuit and original circuit.

- Compute ENF by "flattening" circuit to sum-of-products form without using Boolean identities like $a.a \equiv a$, $a.\bar{a} \equiv 0$, etc.

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Rules for ENF Computation

Primary inputs' ENF \equiv primary input literal

$$\begin{array}{c} a_A \\ b_B \end{array} \quad \begin{array}{c} \text{g} \\ \text{AND} \end{array} \quad a_{A,g} \cdot b_{B,g}$$

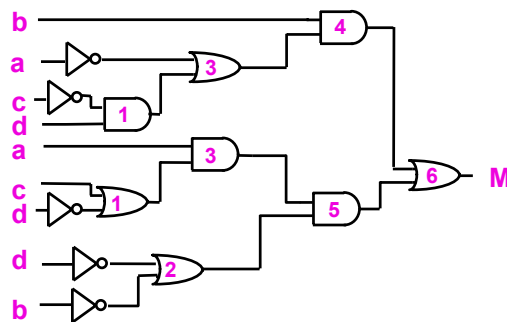
$$\begin{array}{c} a_A \\ b_B \end{array} \quad \begin{array}{c} \text{g} \\ \text{OR} \end{array} \quad a_{A,g} + b_{B,g}$$

$$a_A \quad \begin{array}{c} \text{g} \\ \text{NOT} \end{array} \quad \bar{a}_{A,g}$$

Do not use Boolean identities

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ENF Example

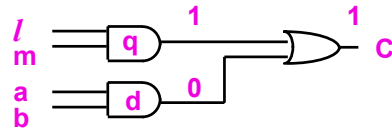


$$\begin{aligned} E_M = & b_{4,6} \bar{a}_{3,4,6} + b_{4,6} \bar{c}_{1,3,4,6} d_{1,3,4,6} \\ & + a_{3,5,6} c_{1,3,5,6} \bar{d}_{2,5,6} + a_{3,5,6} c_{1,3,5,6} \bar{b}_{2,5,6} \\ & + a_{3,5,6} \bar{d}_{1,3,5,6} \bar{d}_{3,5,6} + a_{3,5,6} \bar{d}_{1,3,5,6} \bar{b}_{2,5,6} \end{aligned}$$

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Relatively Essential Vertices (REVs)

In a two-level circuit

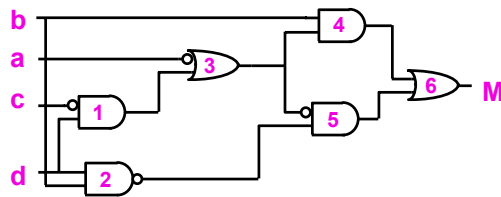


Vector which is relatively essential vertex of q was required for robust path delay fault test for path from l in q

We need a similar concept for multilevel circuits

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Paths and Path-Cube-Complexes



$$E_M = b_{4,6} \bar{a}_{3,4,6} + b_{4,6} \bar{c}_{1,3,4,6} d_{1,3,4,6} \\ + a_{3,5,6} c_{1,3,5,6} \bar{d}_{2,5,6} + a_{3,5,6} c_{1,3,5,6} \bar{b}_{2,5,6} \\ + a_{3,5,6} \bar{d}_{1,3,5,6} \bar{d}_{3,5,6} + a_{3,5,6} \bar{d}_{1,3,5,6} \bar{b}_{2,5,6}$$

Path $a_{3,4,6}$

Path-cube-complex is $b_{4,6} \bar{a}_{3,4,6}$

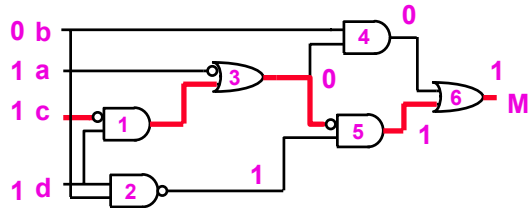
Path $b_{2,5,6}$

Path-cube-complex $a_{3,5,6} c_{1,3,5,6} \bar{b}_{2,5,6} + a_{3,5,6} \bar{d}_{1,3,5,6} \bar{b}_{2,5,6}$

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REVs and Path-Cube-Complexes

Corresponding concept to REV is REV of path cube complex



$$E_M = b_{4,6} \bar{a}_{3,4,6} + b_{4,6} \bar{c}_{1,3,4,6} d_{1,3,4,6} \\ + a_{3,5,6} c_{1,3,5,6} \bar{d}_{2,5,6} + a_{3,5,6} c_{1,3,5,6} \bar{b}_{2,5,6} \\ + a_{3,5,6} \bar{d}_{1,3,5,6} \bar{d}_{3,5,6} + a_{3,5,6} \bar{d}_{1,3,5,6} \bar{b}_{2,5,6}$$

R.E.V. of path-cube-complex of path $c_{1,3,5,6}$ is the

R.E.V. of $a_{3,5,6} c_{1,3,5,6} \bar{d}_{2,5,6} + a_{3,5,6} c_{1,3,5,6} \bar{b}_{2,5,6}$

What is this vertex?

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Associated Karnaugh Map

		00	01	11	10	cd
ab	00					
	01	ab				
	11	ad	bcd		acd	
	10	abd		abc		

R.E.V. of path-cube-complex of path $c_{1,3,5,6}$ is the

R.E.V. of $a_{3,5,6} c_{1,3,5,6} \bar{d}_{2,5,6} + a_{3,5,6} c_{1,3,5,6} \bar{b}_{2,5,6}$

What is the REV?

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Associated Karnaugh Map

		00	01	11	10	cd
ab	00					
	01	ab				
	11	ad	bcd		acd	
	10	abd		abc		

R.E.V. of path-cube-complex of path $c_{1,3,5,6}$ is the

R.E.V. of $a_{3,5,6} c_{1,3,5,6} \bar{d}_{2,5,6} + a_{3,5,6} c_{1,3,5,6} \bar{b}_{2,5,6}$

$$V_2 = 1011$$

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Testability Result

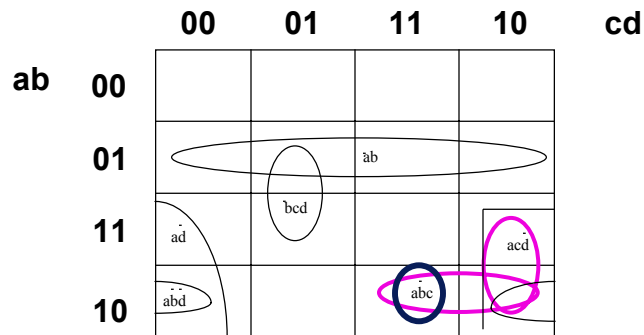
Theorem: (Devadas & Keutzer) A path Π be a path beginning from input l in a multilevel circuit C is testable if and only if there exists a vector pair $\langle V_1, V_2 \rangle$ such that

- 1) V_2 is a relatively essential vertex of the path-cube-complex of Π
- 2) Vertex V_1 distance-1 from V_2 in l is in the OFF-set of C .

Exactly the same as the two-level case!

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Find a test for path $c_{1,3,5,6}$



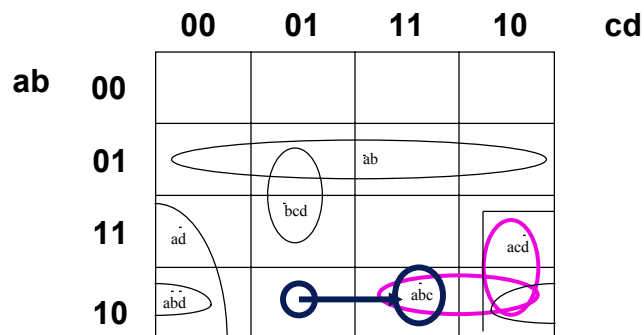
R.E.V. of path-cube-complex of path $c_{1,3,5,6}$ is the

R.E.V. of $a_{3,5,6} c_{1,3,5,6} \bar{d}_{2,5,6} + a_{3,5,6} c_{1,3,5,6} \bar{b}_{2,5,6}$

$$V_2 = 1011, V_1 = ?$$

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Find a test for path $c_{1,3,5,6}$



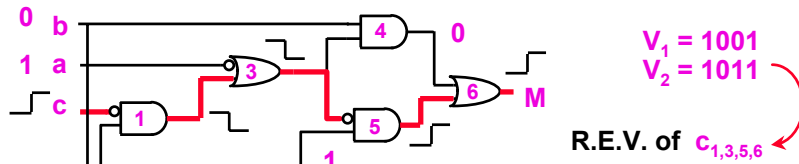
R.E.V. of path-cube-complex of path $c_{1,3,5,6}$ is the

R.E.V. of $a_{3,5,6} c_{1,3,5,6} \bar{d}_{2,5,6} + a_{3,5,6} c_{1,3,5,6} \bar{b}_{2,5,6}$

$$V_2 = 1011, V_1 = 1001$$

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Path Delay Fault Tests



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Find a test for path $b_{2,5,6}$

		00	01	11	10	cd
ab	00					
	01	ab				
	11	ad	bcd		acd	
	10	abd		abc		

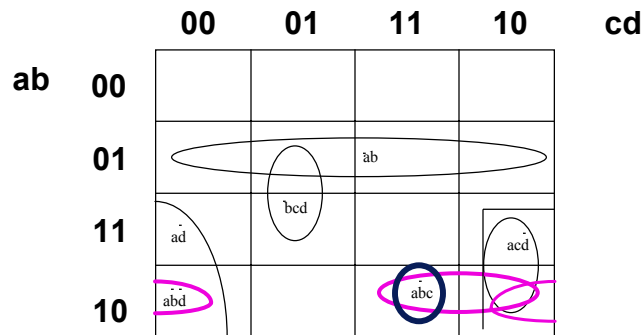
R.E.V. of path-cube-complex of path $\bar{b}_{2,5,6}$ is the

R.E.V. of $a_{3,5,6} d_{1,3,5,6} \bar{b}_{2,5,6} + a_{3,5,6} c_{1,3,5,6} \bar{b}_{2,5,6}$

What is REV?

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Find a test for path $b_{2,5,6}$



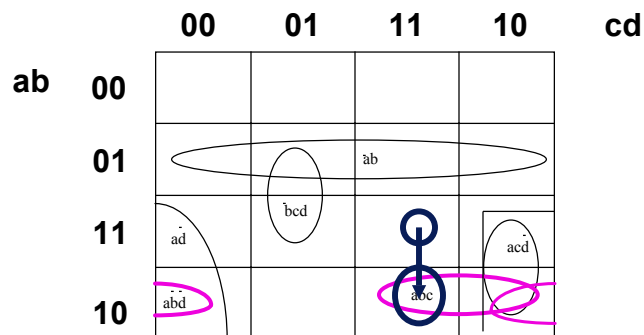
R.E.V. of path-cube-complex of path $\bar{b}_{2,5,6}$ is the

R.E.V. of $a_{3,5,6} d_{1,3,5,6} \bar{b}_{2,5,6} + a_{3,5,6} c_{1,3,5,6} \bar{b}_{2,5,6}$

$V_2 = 1011, V_1 = ?$

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Find a test for path $b_{2,5,6}$



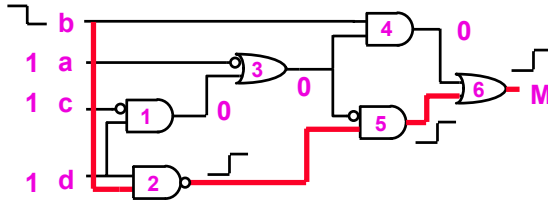
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$V_2 = 1011, V_1 = ?$

50

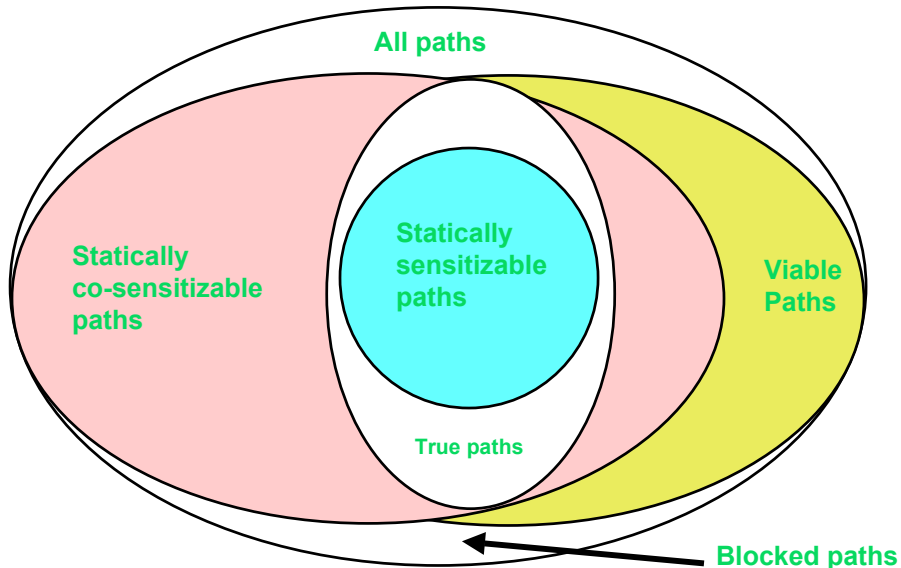
Path Delay Fault Tests



$V_1 = 1111$
 $V_2 = 1011$

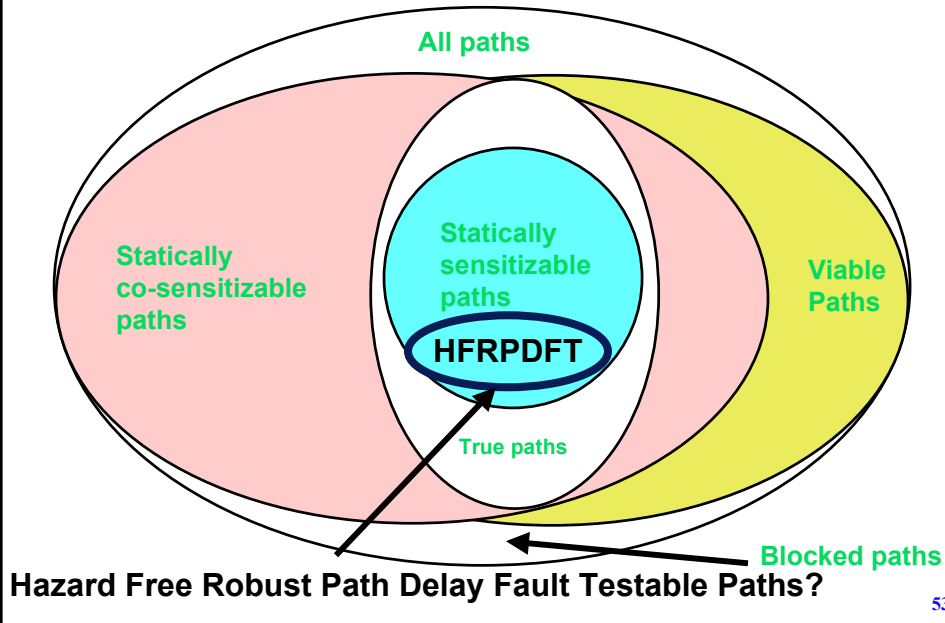
R.E.V. of $\bar{b}_{2,5,6}$

The World of True Paths



Hazard Free Robust Path Delay Fault Testable Paths?

The World of True Paths - 2



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Summary and Conclusions

Primarily a “theoretical lecture” – delay fault testing currently done by *ad hoc* methods

Material does a good job of integrating concepts from:

- 2-level optimization
- Testing
- Path sensitization and static timing analysis

Understand necessary and sufficient conditions for hazard-free delay fault testability

Can translate these into algorithms for producing delay fault tests

Have a constructive procedure for producing 2-level circuits which are multifault testable, delay-fault testable

Algebraic factorization on these circuits preserves testability properties – in extra slides

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Extras

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Synthesizing Testable Circuits

In general, paths in circuits are not hazard-free robust path-delay-fault testable

In a typical circuit perhaps only 15% of the paths have this property

Nevertheless, this is a desirable property to have

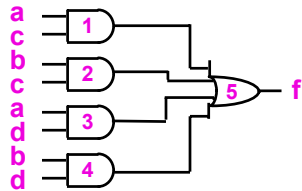
Can we synthesize circuits such that they have this property?

How about multifault testability?

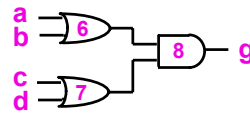
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Key Observation: Algebraic Factorization

ENFs of two-level circuit and *algebraically factored* multilevel circuit are identical except for a renaming of tags.



$$E_f = a_{1,5} c_{1,5} + b_{2,5} c_{2,5} + a_{3,5} d_{3,5} + b_{4,5} d_{4,5}$$



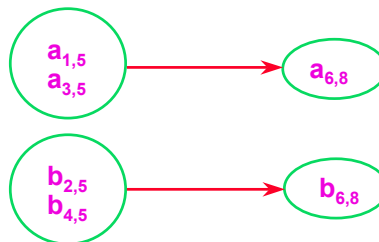
$$E_g = a_{6,8} c_{7,8} + b_{6,8} c_{7,8} + a_{6,8} d_{7,8} + b_{6,8} d_{7,8}$$

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ENF Reducibility

Not only are ENF's syntactically identical there is a many-to-one mapping of tags from two-level circuit to multilevel circuit

$$E_f = a_{1,5} c_{1,5} + b_{2,5} c_{2,5} + a_{3,5} d_{3,5} + b_{4,5} d_{4,5} \quad E_g = a_{6,8} c_{7,8} + b_{6,8} c_{7,8} + a_{6,8} d_{7,8} + b_{6,8} d_{7,8}$$



etc.

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ENF Reducibility Implications

In two-level circuit each path-cube-complex consists of exactly one cube

In multilevel circuit each path-cube-complex can have more than one cube

OFF-sets of circuits are the same, and relatively essential vertices of cubes stay the same.

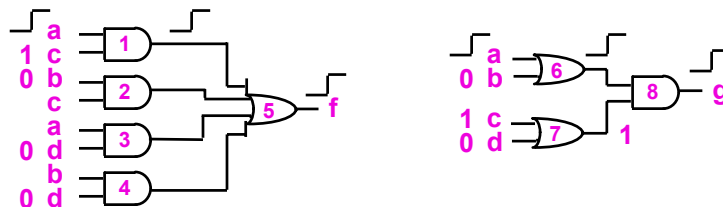
Therefore, testability and test vector sets are maintained.

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Synthesis Procedures

If two-level circuit has full path-delay fault testability, algebraically factored circuit will have full testability.

Same vectors can be applied for delay fault testability.

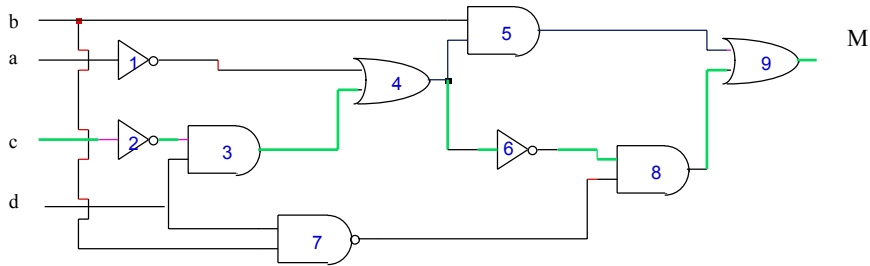


This gives a constructive synthesis procedure for multifault testability and path-delay fault testability

- create 2-level circuit with the property
- algebraically factor

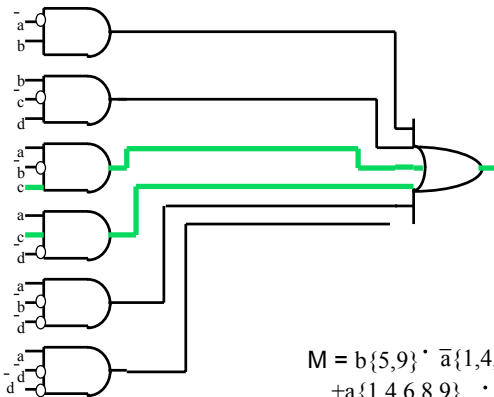
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Multilevel Circuit



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Multiply-out => 2-level circuit and ENF

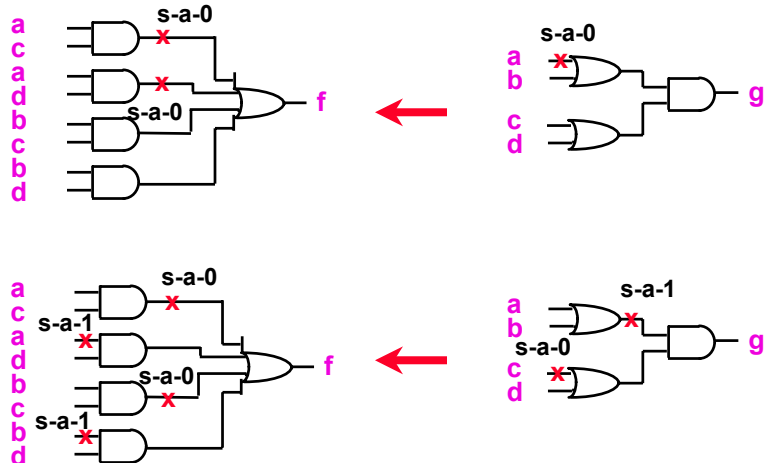


The Equivalent Normal Form (Armstrong - IEEETC, 1966) is a simple sum-of-products representation of the multilevel circuit.

$$\begin{aligned}
 M = & b\{5,9\} \cdot \bar{a}\{1,4,5,9\} + b\{5,9\} \cdot \bar{c}\{2,3,4,5,9\} \cdot d\{3,4,5,9\} \\
 & + a\{1,4,6,8,9\} \cdot \bar{c}\{2,3,4,6,8,9\} \cdot \bar{b}\{7,8,9\} \\
 & + a\{1,4,6,8,9\} \cdot \bar{c}\{2,3,4,6,8,9\} \cdot \bar{d}\{7,8,9\} \\
 & + a\{1,4,6,8,9\} \cdot \bar{d}\{3,4,6,8,9\} \cdot \bar{b}\{7,8,9\} \\
 & + a\{1,3,6,8,9\} \cdot \bar{d}\{3,4,6,8,9\} \cdot \bar{d}\{7,8,9\}
 \end{aligned}$$

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Multifault Equivalence



Test vectors for 2-level cover multifaults in multilevel ckt too

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Summary and Conclusions

Understand necessary and sufficient conditions for hazard-free delay fault testability

Can translate these into algorithms for producing delay fault tests

Have a constructive procedure for producing 2-level circuits which are multifault testable, delay-fault testable

Algebraic factorization on these circuits preserves testability properties

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Path Delay Fault Testability

Not all paths in a prime and irredundant two-level circuit are robustly testable

